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2N5911/5912

PRODUCT SUMMARY					
Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_G Typ (pA)	$\|V_{GS1} - V_{GS2}\|$ Max (mV)
2N5911	–1 to –5	–25	5	–1	10
2N5912	–1 to –5	–25	5	–1	15

FEATURES

- Two-Chip Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 1 pA
- Low Noise
- High CMRR: 85 dB

BENEFITS

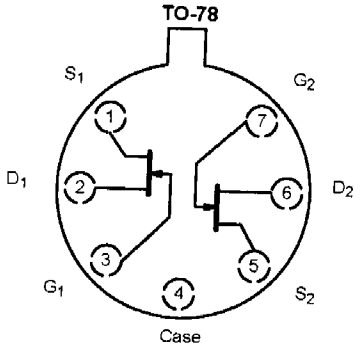
- Minimum Parasitics Ensuring Maximum High-Frequency Performance
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

APPLICATIONS

- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High Speed Comparators
- Impedance Converters

DESCRIPTION

The 2N5911/5912 are matched pairs of JFETs mounted in a TO-78 package. This two-chip design reduces parasitics and gives better performance at high frequencies while ensuring extremely tight matching.



ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage	–25 V
Gate-Gate Voltage	±80 V
Gate Current	50 mA
Lead Temperature ($1/16$" from case for 10 sec.)	300°C
Storage Temperature	–65 to 200°C
Operating Junction Temperature	–55 to 150°C

Power Dissipation :	Per Side[a]	367 mW
	Total[b]	500 mW

Notes
a. Derate 3 mW/°C above 25°C
b. Derate 4 mW/°C above 25°C

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions	Typ[a]	Limits 2N5911 Min	Limits 2N5911 Max	Limits 2N5912 Min	Limits 2N5912 Max	Unit
Static								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = –1 µA, V_{DS} = 0 V	–35	–25		–25		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 nA	–3.5	–1	–5	–1	–5	
Saturation Drain Current[b]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	7	40	7	40	mA
Gate Reverse Current	I_{GSS}	V_{GS} = –15 V, V_{DS} = 0 V	–1		–100		–100	pA
		T_A = 150°C	–2		–250		–250	nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	–1		–100		–100	pA
		T_A = 125°C	–0.3		–100		–100	nA
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, I_G = 5 mA	–1.5	–0.3	–4	–0.3	–4	V
Gate-Source Forward Voltage[c]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					
Dynamic								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	6	5	10	5	10	mS
Common-Source Output Conductance	g_{os}		70		100		100	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 100 MHz	5.8	5	10	5	10	mS
Common-Source Output Conductance	g_{os}		90		150		150	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	3		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1		1.2		1.2	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 5 mA, f = 10 kHz	4		20		20	$\frac{nV}{\sqrt{Hz}}$
Noise Figure	NF	R_G = 100 kΩ	0.1		1		1	dB
Matching								
Differential Gate-Source Voltage	$\lvert V_{GS1} - V_{GS2} \rvert$	V_{DG} = 10 V, I_D = 5 mA	4		10		15	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 5 mA, T_A = –55 to 125°C	15		20		40	µV/°C
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.98	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DS} = 10 V, I_D = 5 mA, f = 1 kHz	0.98	0.95	1	0.95	1	
Differential Gate Current	$\lvert I_{G1} - I_{G2} \rvert$	V_{DG} = 10 V, I_D = 5 mA, T_A = 125°C	0.005		20		20	nA
Common Mode Rejection Ratio[c]	CMRR	V_{DG} = 5 to 10 V, I_D = 5 mA	85					dB

Notes
a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. Pulse test: PW ≤ 300 µs duty cycle ≤ 3%.
c. This parameter not registered with JEDEC.