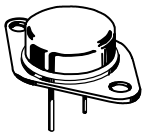
2N6251

High Voltage NPN Silicon Power Transistors

15 AMPERE
POWER TRANSISTOR
NPN SILICON
350 VOLTS
175 WATTS

. . . designed for high voltage inverters, switching regulators and line operated amplifier applications. Especially well suited for switching power supply applications.

- High Voltage Breakdown Rating
- Low Saturation Voltages
- Fast Switching Capability
- High $E_{S/b}$ Energy Handling Capability



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage (1)	$V_{CEO(sus)}$	350	Vdc
Collector–Emitter Voltage (1)	$V_{CER(sus)}$	375	Vdc
Collector–Base Voltage (1)	V_{CB}	450	Vdc
Emitter–Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous** — Peak	I_C I_{CM}	15 30	Adc
Base Current — Continuous (1) — Peak	I_B I_{BM}	10 20	Adc
Emitter Current — Continuous — Peak	I_E I_{EM}	25 50	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C*	P_D	175 100 1.0	Watts W/°C
Operating and Storage Junction (1) Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8” from Case for 5 Seconds	T_L	275	°C

(1) Indicates JEDEC Registered Data.
** JEDEC Registered Value is 10 A, Motorola Guaranteed Value is 15 A.

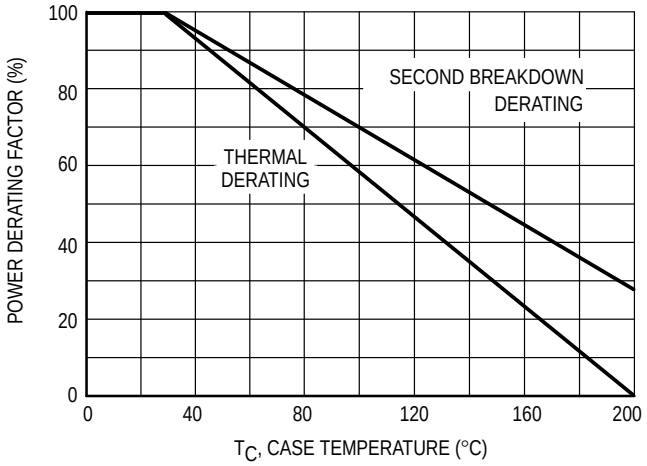


Figure 1. Power Derating

REV 1

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 200 mA, I_B = 0)		$V_{CEO(sus)}$	350	—	Vdc
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 200 mA)		$V_{CER(sus)}$	375	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CER}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CER}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)		I_{CEV}	 — —	 5.0 10	mAdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 225 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)		I_{CEO}	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased t = 1.0s (non–repetitive)	(V_{CE} = 30 V) (V_{CE} = 100 V)	$I_{S/b}$	5.8 0.3	— —	Vdc
Second Breakdown Energy with base reverse biased (Table 1) (I_C = 10 A, $V_{BE(off)}$ = 4.0 Vdc, L = 50 μH)		$E_{S/b}$	2.5	—	mJ
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	6.0	50	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.67 Adc)		$V_{CE(sat)}$	—	1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.25 Adc) (I_C = 10 Adc, I_B = 1.67 Adc)		$V_{BE(sat)}$	—	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	2.5	—	MHz
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Rise Time	(V_{CC} = 200 Vdc, I_C = 10 A, Duty Cycle ≤ 2.0%, t_p = 100 μs) (I_{B1} = I_{B2} = 1.67 Adc)	t_r	—	2.0	μs
Storage Time		t_s	—	3.5	μs
Fall Time		t_f	—	1.0	μs

* Indicates JEDEC Registered Data.

(1) Measured on a curve tracer (60 Hz full–wave rectified sine wave).

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	$V_{CER(sus)}$	$E_{S/b}$	RESISTIVE SWITCHING
INPUT CONDITIONS	+6.0 V, 0, 39, 1, 2	+6.0 V, 0, 39, 51, 1, 2	I_{B1} = 2.0 A, +10 V, 0, 50, 1, 50, 4 V, 2	+15 V, 50 µF, TIP41B, 4.7, 51, 51, 0.02 µF, 1, 2
CIRCUIT VALUES	L_{coil} = 42 mH R_{coil} = 0.7 Ω, f_o = 60 Hz V_{CC} = 0 to 50 V	L_{coil} = 14 mH R_{coil} = 0.05 Ω V_{CC} = 0 to 50 V f_o = 60 Hz	L_{coil} = 50 µH, V_{CC} = 11.5 V R_{coil} = 0.2 Ω	V_{CC} = 200 V R_L = 20 Ω
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT: TUT, 1N4937, R_{coil}, L_{coil}, V_{CL}, R_S 0.1, V_{CC}, 1, 2	OUTPUT WAVEFORMS: I_C, $I_{C(pk)}$, t, t_1, t_f, V_{CE}, t	t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}\ (I_{Cpk})}{V_{CC}}$	RESISTIVE TEST CIRCUIT: +200 V, 20, DC CURRENT PROBE, 1, TUT, 3, 2, 25, −6.0 V

NOTE: SET $I_{C(pk)}$ TO OBTAIN I_C = 200 mA AT $V_{CEO(sus)}$ EQUAL TO RATED VALUE.
ADJUST V_{Clamp} VOLTAGE FOR $V_{CEO(sus)}$ RATED VALUE.

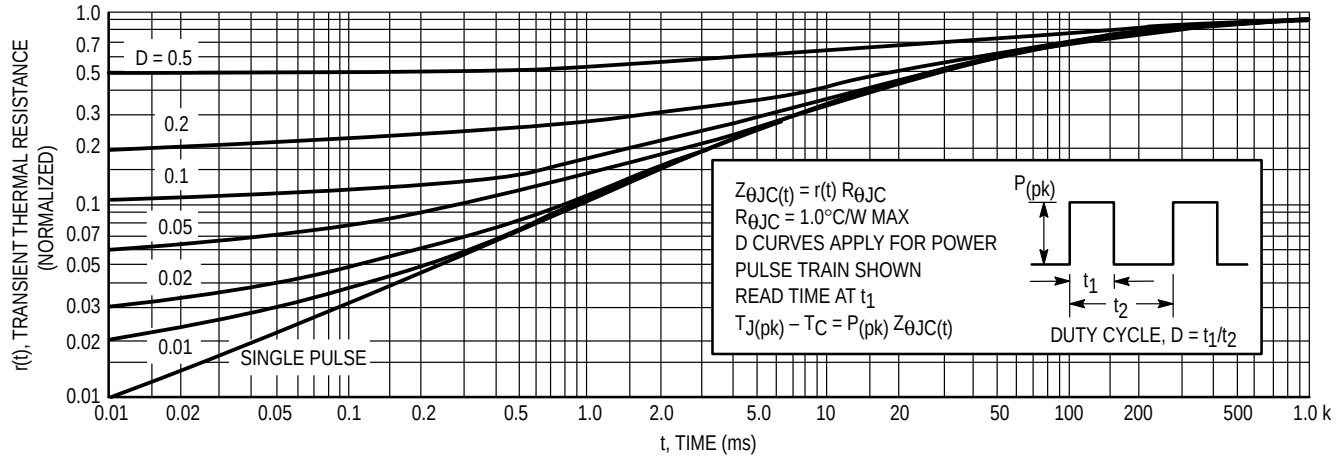


Figure 2. Thermal Response

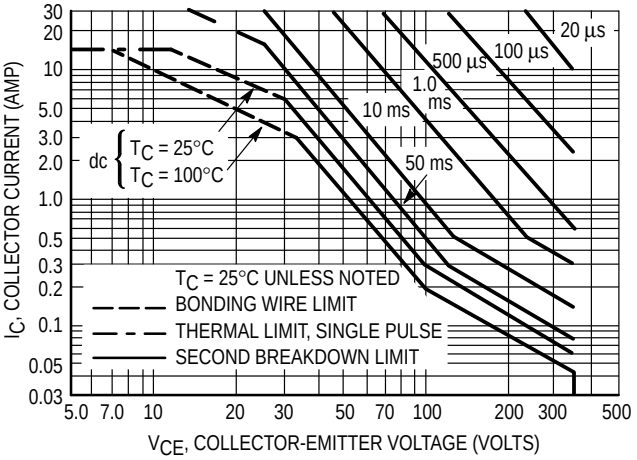


Figure 3. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on T_C = 25°C. $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltage shown on Figure 3 may be found at any case temperature by using the appropriate curve on Figure 1.

$T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

DC CHARACTERISTICS

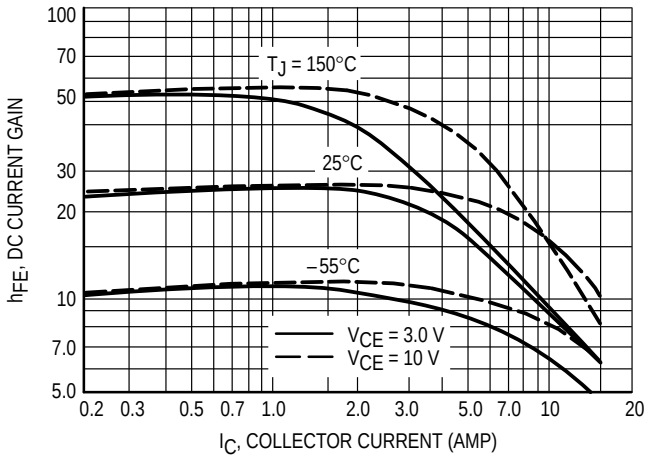


Figure 4. DC Current Gain

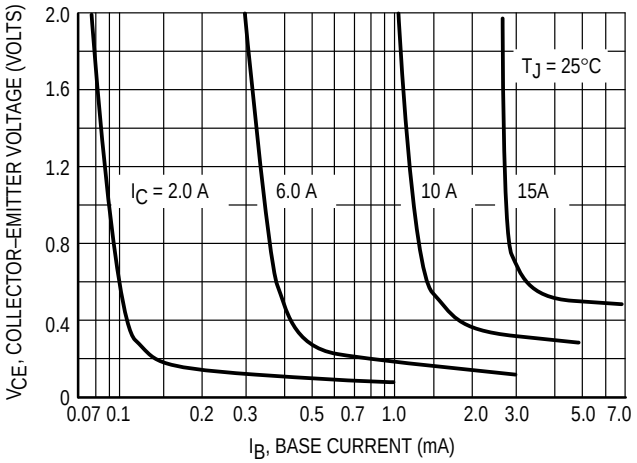


Figure 5. Collector Saturation Region

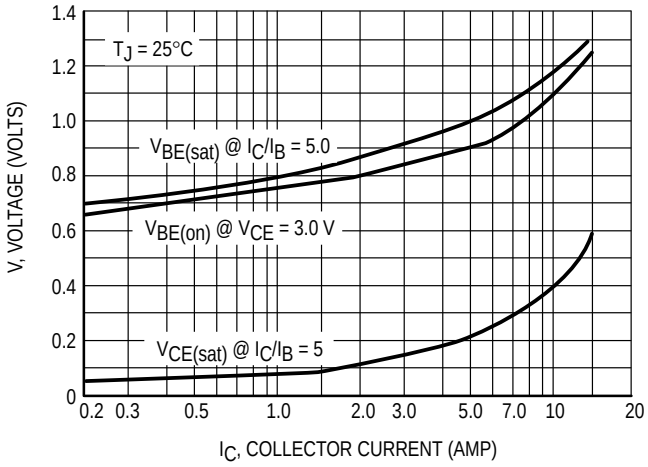


Figure 6. "On" Voltagae

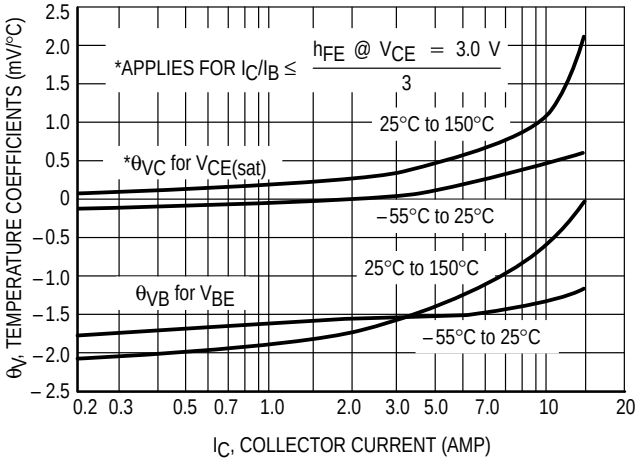


Figure 7. Temperature Coefficients

RESISTIVE SWITCHING PERFORMANCE

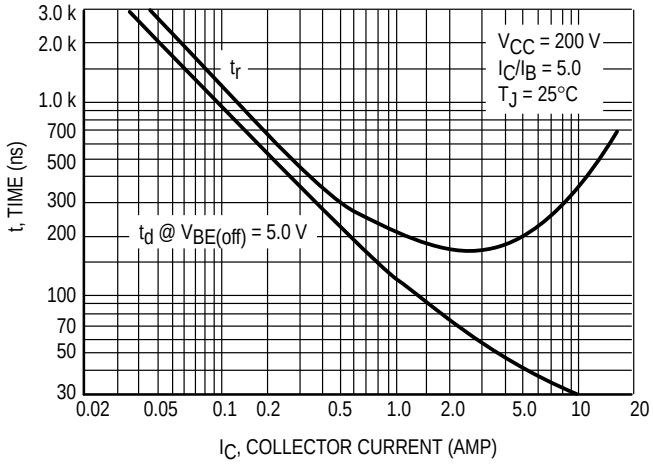


Figure 8. Turn-on Time

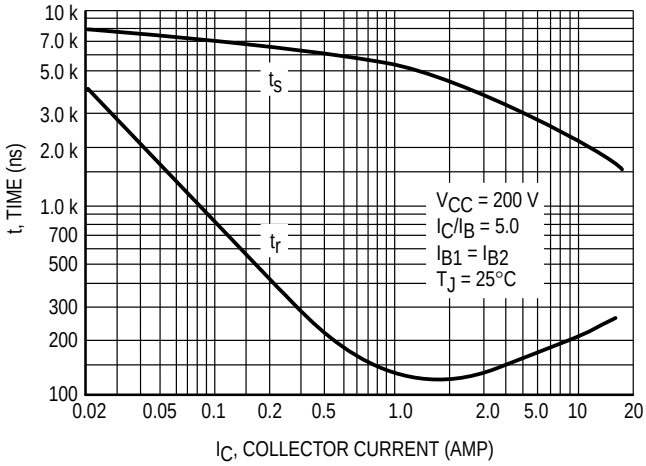
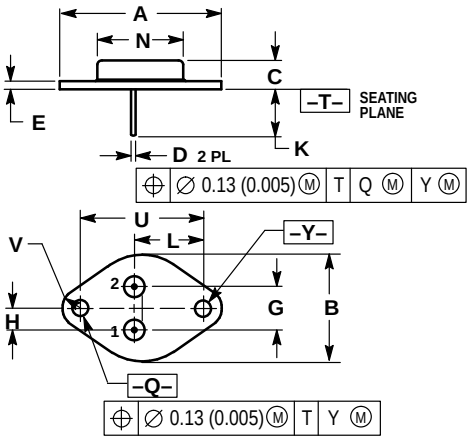


Figure 9. Turn-off Time

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 1–07
TO–204AA (TO–3)
ISSUE Z

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