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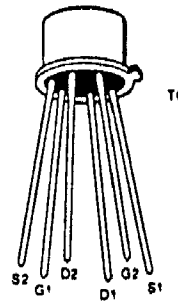
Dual N-Channel JFET Low Noise Amplifier

2N6483 – 2N6485

FEATURES

- Ultra Low Noise
- High CMRR
- Low Offset
- Tight Tracking

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise specified)

Gate-Source or Gate-Drain Voltage (Note 1) . . . . . -50V
Gate-Gate Voltage . . . . . ±50V
Gate Current (Note 1) 50mA
Storage Temperature Range . . . . . -65°C to +200°C
Operating Temperature Range . . . . . -55°C to +175°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C

	One Side	Both Sides
Power Dissipation	250mW	400mW
Derate above 25°C	1.7mW/°C	2.7mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
2N6483	Hermetic TO-71	-55°C to +175°C
2N6484	Hermetic TO-71	-55°C to +175°C
2N6485	Hermetic TO-71	-55°C to +175°C
X2N6485	Sorted Chips in Carriers	-55°C to +175°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
I_{GSS}	Gate Reverse Current		-200	pA	V_{GS} = -30V, V_{DS} = 0
			-200	nA	T_A = 150°C
BV_{GSS}	Gate Reverse Breakdown Voltage	-50		V	I_G = -1µA, V_{DS} = 0
V_P	Gate-Source Pinch Off Voltage	-0.7	-4.0		V_{DS} = 20V, I_D = 1nA
I_{DSS}	Drain Current at Zero Gate Voltage (Note 2)	0.5	7.5	mA	V_{DS} = 20V, V_{GS} = 0
g_{fs}	Common-Source Forward Transconductance (Note 2)	1000	4000	µs	V_{DS} = 20V, V_{GS} = 0, f = 1kHz (Note 6)
g_{oss}	Common-Source Output Conductance				
C_{iss}	Common-Source Input Capacitance		20	pF	V_{DS} = 20V, V_{GS} = 0, f = 1MHz (Note 6)
C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		
I_G	Gate Current		100	pA	V_{DG} = 20V, I_D = 200µA, (Note 6)
			100	nA	T_A = 150°C
V_{GS}	Gate Source Voltage	0.2	3.8	V	V_{DG} = 20V, I_D = 200µA
g_{fs}	Common-Source Forward Transconductance	500	1500	µs	V_{DG} = 20V, I_D = 200µA, f = 1kHz
g_{os}	Common-Source Output Conductance		1		V_{DG} = 20V, I_D = 200µA
$\overline{e_n}$	Equivalent Input Noise Voltage (Note 6)		10	nV/√Hz	V_{DS} = 20V, I_D = 200µA, f = 10Hz
			5		V_{DS} = 20V, I_D = 200µA, f = 1kHz

NOTES: 1. Per transistor
2. Pulse test required; pulse width = 2ms

MATCHING CHARACTERISTICS (Continued) (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	2N6483 MIN	2N6483 MAX	2N6484 MIN	2N6484 MAX	2N6485 MIN	2N6485 MAX	UNITS	TEST CONDITIONS
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage	0.95	1	0.95	1	0.95	1		V_{DS} = 20V, V_{GS} = 0 (Note 4)
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current		10		10		10	nA	V_{DG} = 20V, I_D = 200µA, T_A = +125°C
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.97	1	0.97	1	0.95	1		V_{DG} = 20V, I_D = 200µA, f = 1kHz (Note 4)
$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance (Note 6)		0.1		0.1		0.1	µs	V_{DG} = 20V, I_D = 200µA, f = 1kHz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DG} = 20V, I_D = 200µA
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		5		10		25	µV/°C	V_{DG} = 20V, I_D = 200µA, T_A = -55°C to +125°C
CMRR	Common Mode Rejection Ratio (Note 6)	100		100		90		dB	V_{DD} = 10 to 20V, I_D = 200µA (Note 5)