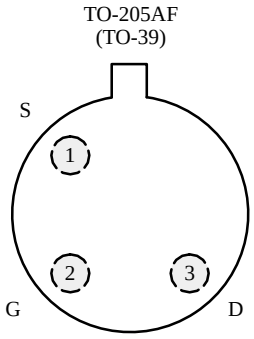
2N6851

P-Channel Enhancement-Mode Transistor

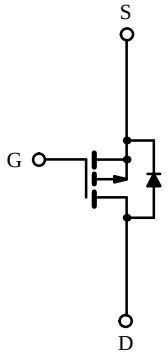
Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–200	0.80	–4.0

Parametric limits in accordance with MIL-S-19500/564 where applicable.



Top View



P-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–200	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	–4.0	A
	T_C = 100°C		–2.4	
Pulsed Drain Current		I_{DM}	–20	
Avalanche Current		I_{AR}	–3.1	
Maximum Power Dissipation	T_C = 25°C	P_D	25	W
	T_C = 100°C		10	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient	R_{thJA}	175	°C/W
Maximum Junction-to-Case	R_{thJC}	5.0	

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1490.

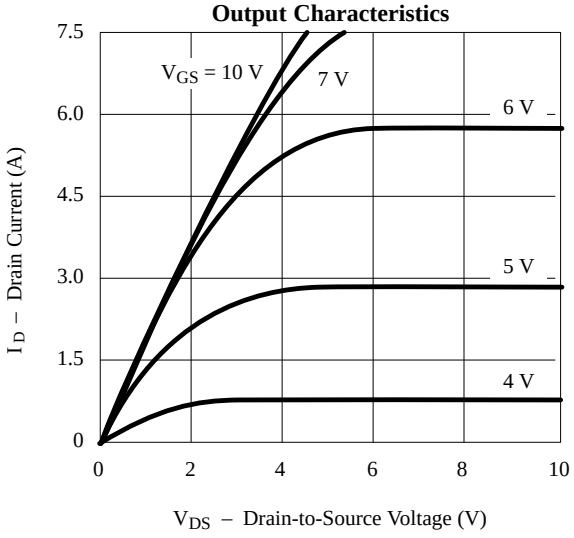
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Limit			Unit
			Min	Typ[a]	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = –1000 µA	–200			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250 µA	–2.0		–4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –160 V, V_{GS} = 0 V			–25	µA
		V_{DS} = –160 V, V_{GS} = 0 V, T_J = 125°C			–250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = –3.3 V, V_{GS} = –10 V	–4.0			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = –10 V, I_D = –2.4 A		0.50	0.80	Ω
		V_{GS} = –10 V, I_D = –2.4 A, T_J = 125°C		1.0	1.6	
Forward Transconductance[b]	g_{fs}	V_{DS} = –15 V, I_D = –2.4 A	2.2	2.	6.6	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = –25 V, f = 1 MHz		625		pF
Output Capacitance	C_{oss}			280		
Reverse Transfer Capacitance	C_{rss}			105		
Total Gate Charge[c]	Q_g	V_{DS} = –100 V, V_{GS} = –10 V, I_D = –4.0 A	14.7	24	34.8	nC
Gate-Source Charge[c]	Q_{gs}		0.5	3.4	6.1	
Gate-Drain Charge[c]	Q_{gd}		3.3	13.5	20.1	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = –100 V, R_L = 39 Ω I_D ≅ –2.4 A, V_{GEN} = –10 V, R_G = 7.5 Ω		9	50	ns
Rise Time[c]	t_r			50	100	
Turn-Off Delay Time[c]	$t_{d(off)}$			32	80	
Fall Time[c]	t_f			38	80	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				–4.0	A
Pulsed Current	I_{SM}				–20	
Diode Forward Voltage[b]	V_{SD}	I_F = –4.0 A, V_{GS} = 0 V	–0.8		–2.0	V
Reverse Recovery Time	t_{rr}	I_F = –4.0 A, di/dt = 100 A/µs		160	400	ns
Reverse Recovery Charge	Q_{rr}			1.6		µC

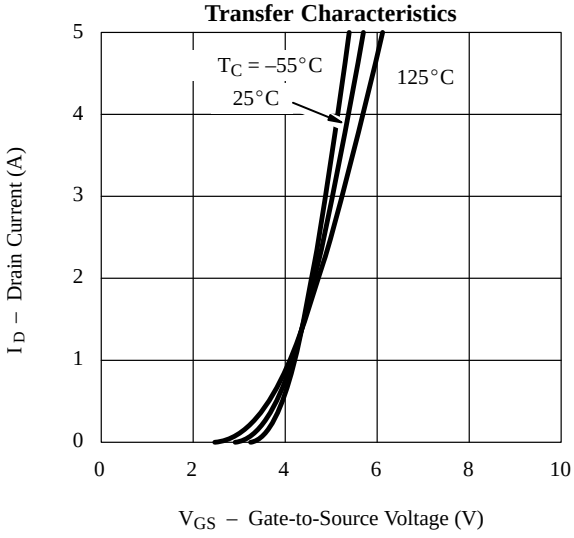
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

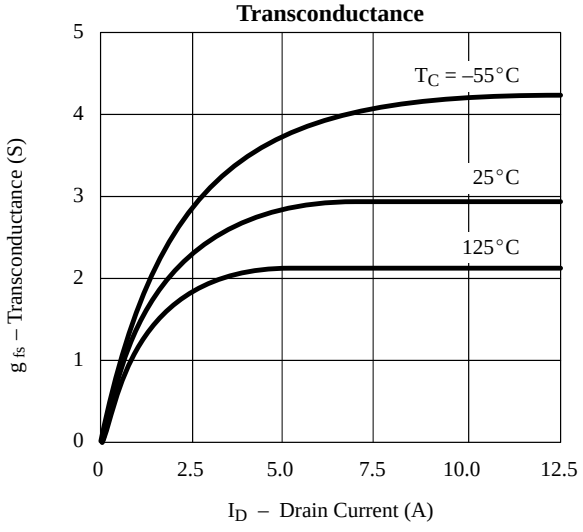
Output Characteristics



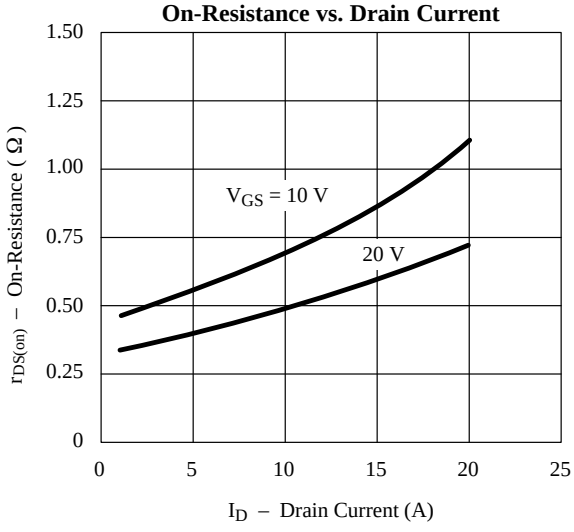
Transfer Characteristics



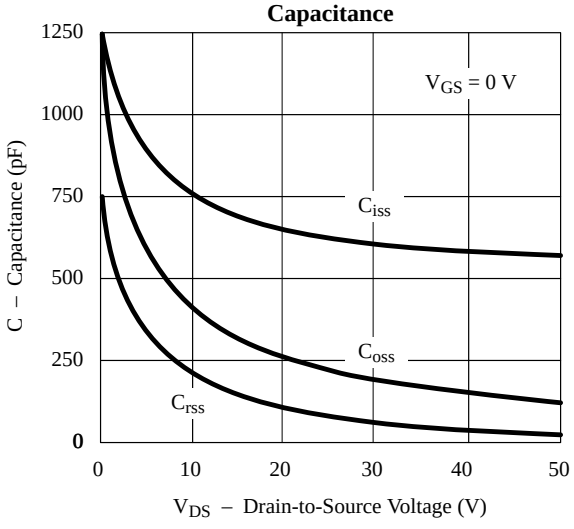
Transconductance



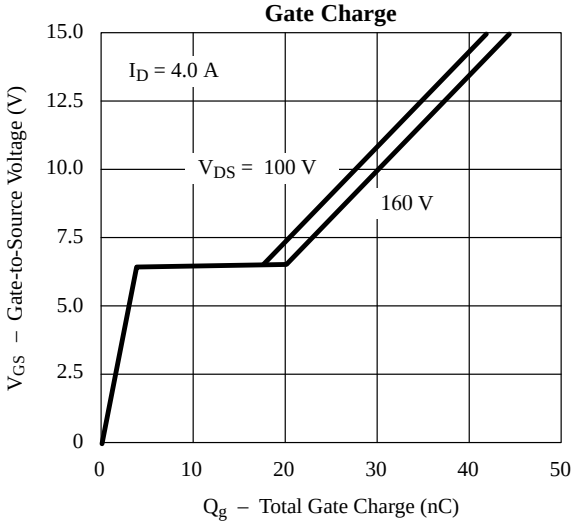
On-Resistance vs. Drain Current



Capacitance

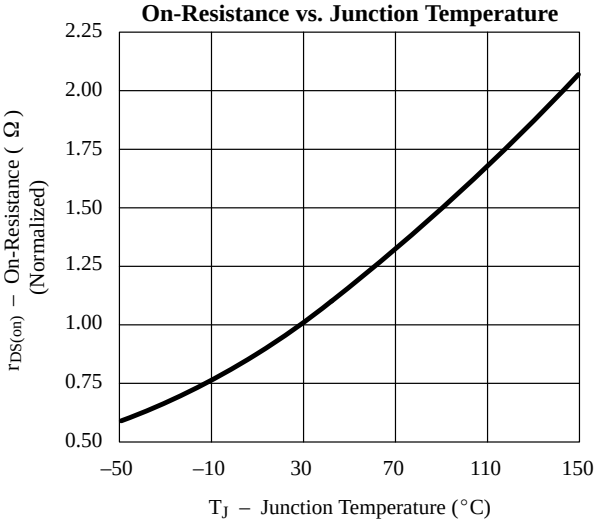


Gate Charge

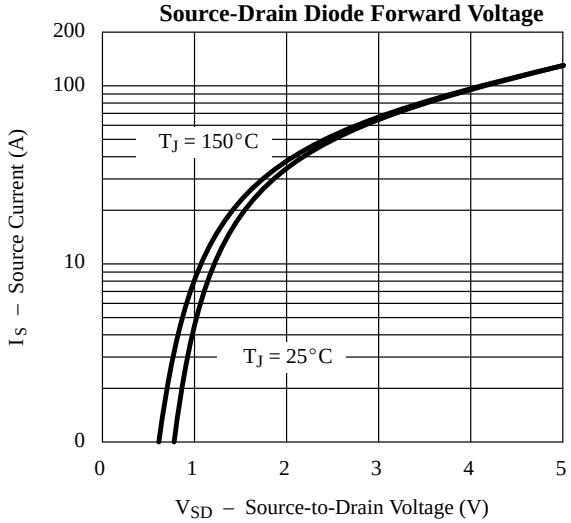


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

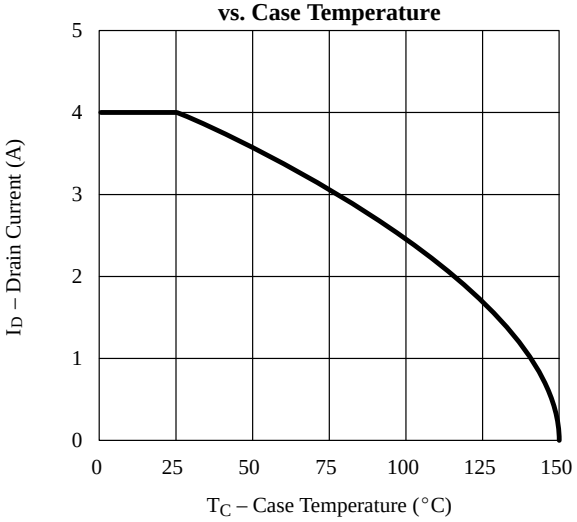


Source-Drain Diode Forward Voltage

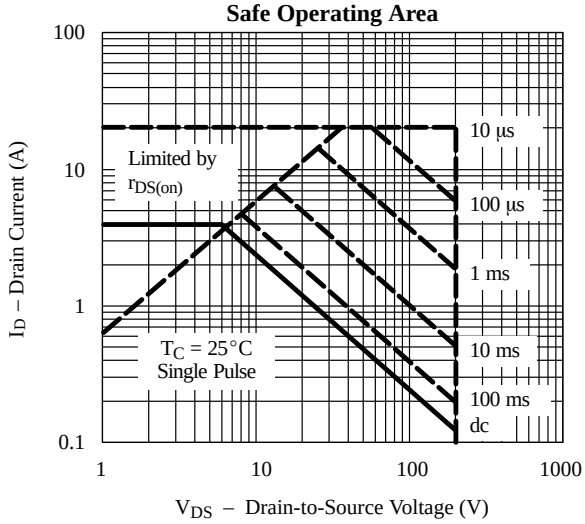


Thermal Ratings

Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case