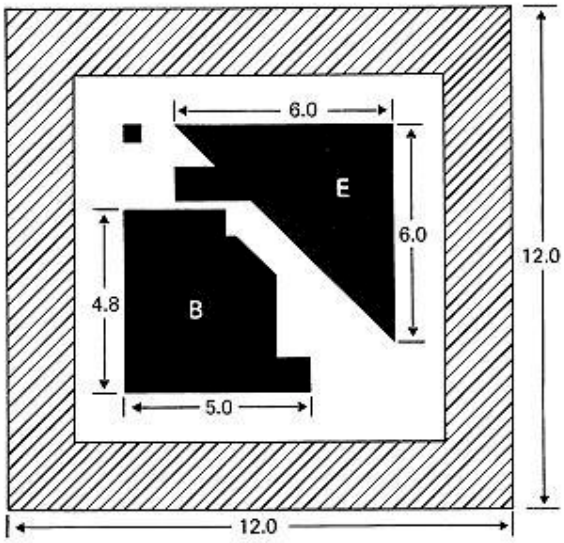
DIONICS INC.
65 RUSHMORE ST., WESTBURY, N.Y. 11590 516•997•7474

2N918

NPN SILICON
HIGH FREQUENCY TRANSISTOR CHIPS DESIGNED
FOR HYBRID CIRCUIT APPLICATIONS



Dimensions in Mils

Silicon Aluminum Oxide

- Chip Thickness—6 Mils ±1 Mil
- Min. Dimension Across Bonding Pads—4.0 Mils
- Min. Separation Between Bonding Pads—1.0 Mils
- Distance from Bonding Pads to Edge of Chip—2.25 Mils

Detailed Specifications on Reverse Side.

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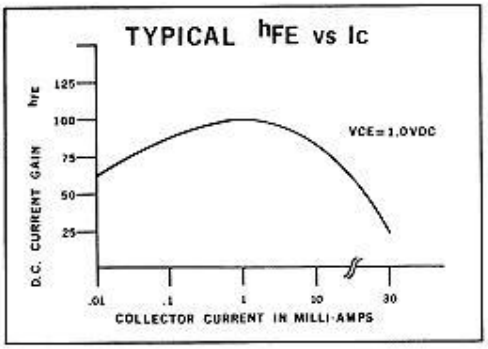
LOW LEAKAGE CHARACTERISTICS • OVERSIZED BONDING PADS
NO BETA DEGRADATION DURING PROLONGED HIGH TEMPERATURE ASSEMBLY

Unique surface stabilization processing results in lower leakage currents and improved beta stability. These devices are therefore free from the beta degradation frequently encountered during the extended high temperature assembly operations required for complex hybrid construction.

The large area bonding pads are positioned for maximum flexibility of substrate layout.

Chips are gold backed for eutectic die-attach, and have aluminum bonding pads for all conventional wire bonding techniques.



← 100% Probe Tested to These Parameters @ 25°C → ← Guaranteed → (tested on sample basis)

	h_{FE} @V_{CE} = 1V, I_C = 3mA	V_{CBO} Volts Min. @I_C = 1μA, I_E = 0	V_{CEO} Volts Min. @I_C = 3mA, I_B = 0	V_{EBO} Volts Min. @I_B = 10μA, I_C = 0	I_{CBO} nA Max. @V_{CB} 15V, I_E = 0	V_{CE} (SAT.) Volts Max. @I_C = 10mA, I_B = 1mA	C_{CB} pF Max. @V_{CB} 10V, I_E = 0, f = 140KHz	f_t MHz Min. @ I_C = 4mA, V_{CE} = 10V, f = 100 MHz
2N918	20 MIN	30	15	3	10	0.4	1.7	600

Demensional Drawing on Reverse Side