

2SD1350, 2SD1350A

Silicon NPN triple diffusion planar type

For high breakdown voltage switching

■ Features

- High collector-base voltage (Emitter open) V_{CBO}
- Large collector power dissipation P_C
- Low collector-emitter saturation voltage $V_{CE(sat)}$
- M type package, allowing easy automatic and manual insertion as well as stand-alone fixing to the printed circuit board.

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

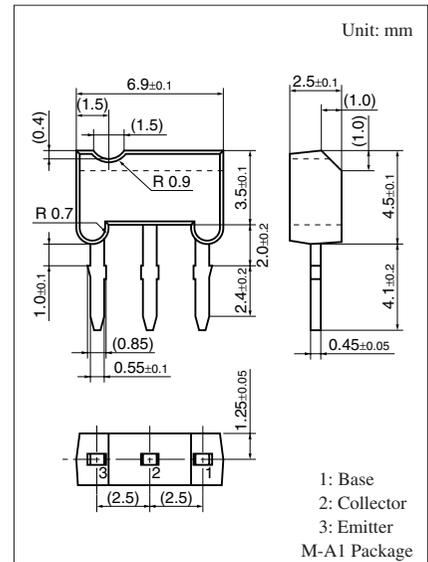
Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	400 600	V
Collector-emitter voltage (Base open)	V_{CEO}	400 500	V
Emitter-base voltage (Collector open)	V_{EBO}	5	V
Collector current	I_C	500	mA
Peak collector current	I_{CP}	1	A
Collector power dissipation *	P_C	1	W
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

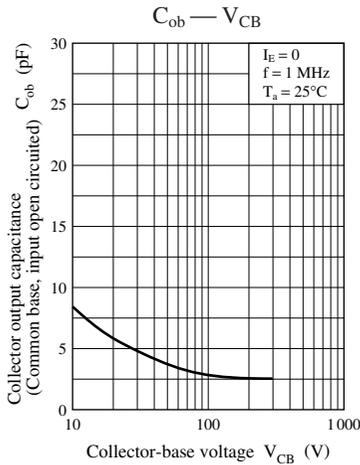
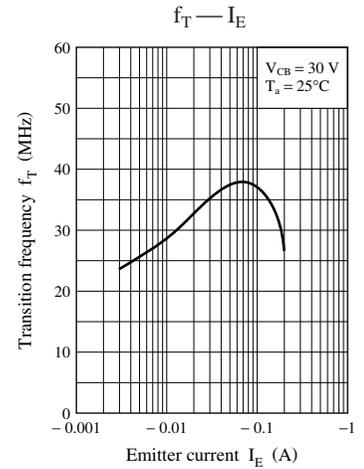
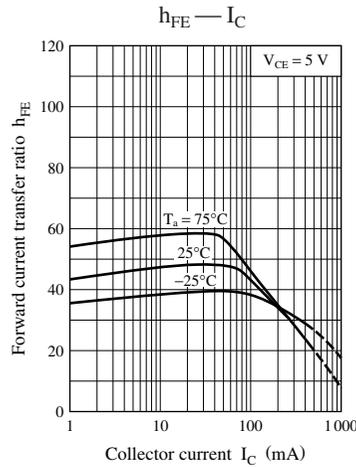
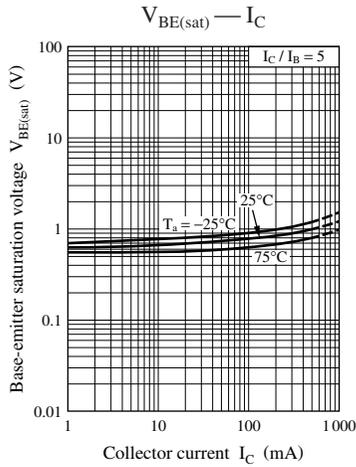
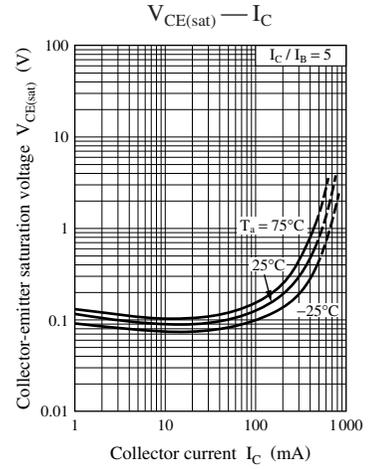
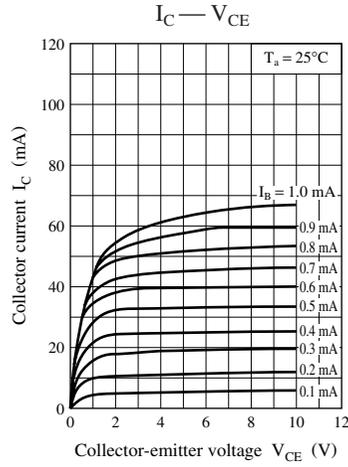
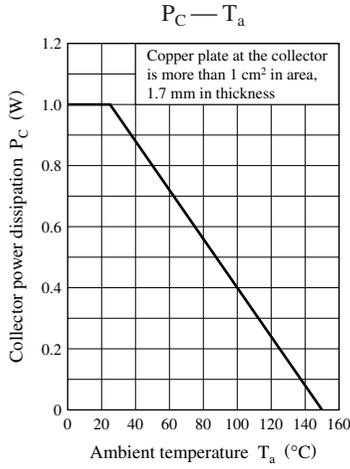
Note) *: Printed circuit board: Copper foil area of 1 cm² or more, and the board thickness of 1.7 mm for the collector portion

■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	V_{CBO}	$I_C = 100 \mu\text{A}$, $I_E = 0$	400 600			V
Collector-emitter voltage (Base open)	V_{CEO}	$I_C = 500 \mu\text{A}$, $I_B = 0$	400 500			V
Emitter-base voltage (Collector open)	V_{EBO}	$I_E = 100 \mu\text{A}$, $I_C = 0$	5			V
Forward current transfer ratio	h_{FE}	$V_{CE} = 5 \text{ V}$, $I_C = 30 \text{ mA}$	30			—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = 250 \text{ mA}$, $I_B = 50 \text{ mA}$			1.5	V
Base-emitter saturation voltage	$V_{BE(sat)}$	$I_C = 250 \text{ mA}$, $I_B = 50 \text{ mA}$			1.5	V
Transition frequency	f_T	$V_{CB} = 30 \text{ V}$, $I_E = -20 \text{ mA}$, $f = 200 \text{ MHz}$		55		MHz
Collector output capacitance (Common base, input open circuited)	C_{ob}	$V_{CB} = 30 \text{ V}$, $I_E = 0$, $f = 1 \text{ MHz}$			7	pF
Turn-on time	t_{on}	$V_{CC} = 200 \text{ V}$, $I_C = 100 \text{ mA}$ $I_{B1} = 10 \text{ mA}$, $I_{B2} = -10 \text{ mA}$		0.4		μs
Fall time	t_f	$V_{CC} = 200 \text{ V}$, $I_C = 100 \text{ mA}$ $I_{B1} = 10 \text{ mA}$, $I_{B2} = -10 \text{ mA}$		0.7		μs
Storage time	t_{stg}	$V_{CC} = 200 \text{ V}$, $I_C = 100 \text{ mA}$ $I_{B1} = 10 \text{ mA}$, $I_{B2} = -10 \text{ mA}$		3.6		μs

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.





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