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P1 98.2

MOS FIELD EFFECT POWER TRANSISTOR  
**2SJ303**

SWITCHING  
 P-CHANNEL POWER MOS FET  
 INDUSTRIAL USE

**DESCRIPTION**

The 2SJ303 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

**FEATURES**

- Low On-state Resistance.  
 $R_{DS(on)} \leq 0.1 \Omega$  ( $V_{GS} = -10 \text{ V}$ ,  $I_D = -7 \text{ A}$ )  
 $R_{DS(on)} \leq 0.24 \Omega$  ( $V_{GS} = -4 \text{ V}$ ,  $I_D = -6 \text{ A}$ )
- Low  $C_{iss}$   $C_{iss} = 1\ 200 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diode
- Isolated TO-220 Package

**QUALITY GRADE**

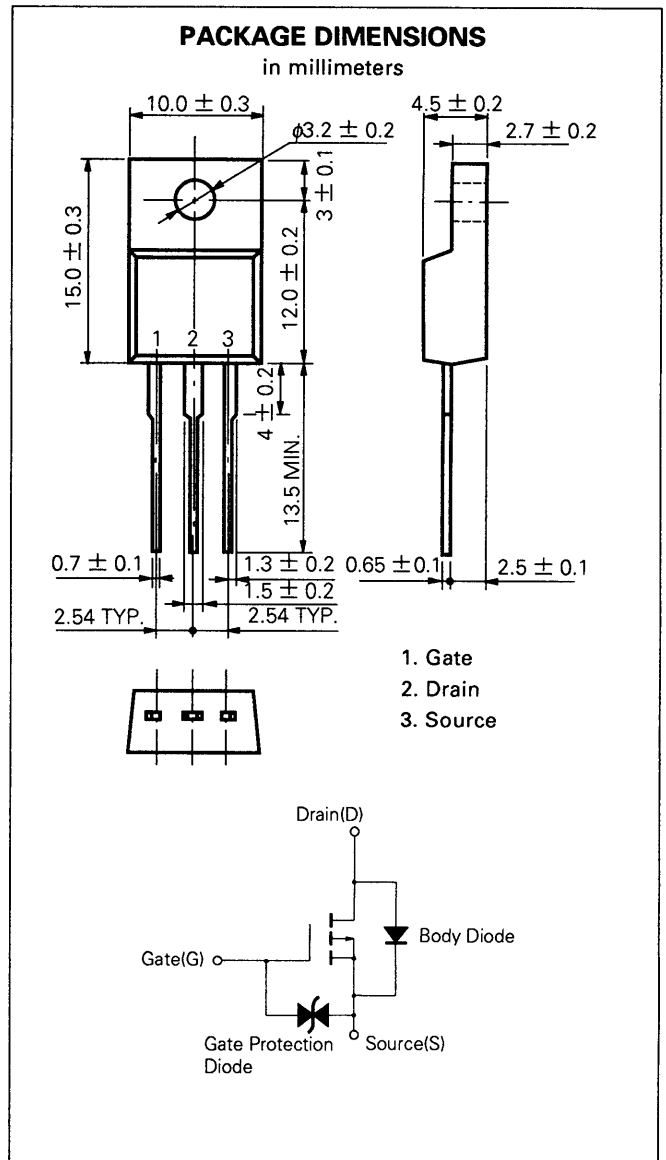
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

**ABSOLUTE MAXIMUM RATINGS ( $T_a = 25 \text{ }^\circ\text{C}$ )**

Drain to Source Voltage	$V_{DS}$	-60	V
Gate to Source Voltage	$V_{GS}$	-20, +10	V
Drain Current (DC)	$I_{D(DC)}$	$\mp 14$	A
Drain Current (pulse)	$I_{D(pulse)*}$	$\mp 56$	A
Total Power Dissipation ( $T_c = 25 \text{ }^\circ\text{C}$ )	$P_{T1}$	35	W
Total Power Dissipation ( $T_a = 25 \text{ }^\circ\text{C}$ )	$P_{T2}$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

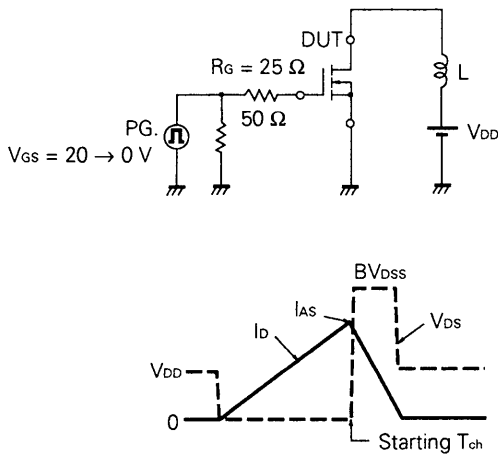
\*  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1 \%$



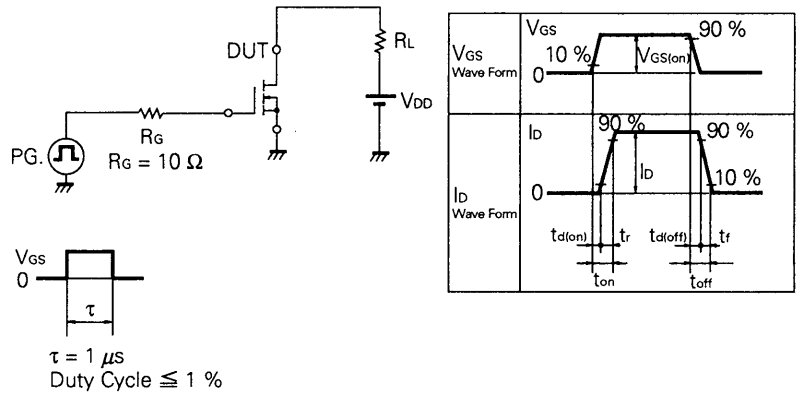
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		75	100	mΩ	V <sub>GS</sub> = -10 V, I <sub>b</sub> = -7 A
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		130	240	mΩ	V <sub>GS</sub> = -4.0 V, I <sub>b</sub> = -6 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	-1.0		-2.0	V	V <sub>DS</sub> = -10 V, I <sub>b</sub> = -1 mA
Forward Transfer Admittance	y <sub>fs</sub>	5.0			S	V <sub>DS</sub> = -10 V, I <sub>b</sub> = -7 A
Drain Leakage Current	I <sub>DSS</sub>			-10	μA	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		1200		pF	V <sub>DS</sub> = -10 V V <sub>GS</sub> = 0 f = 1 MHz
Output Capacitance	C <sub>oss</sub>		670		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		290		pF	
Turn-On Delay Time	t <sub>d(on)</sub>		30		ns	V <sub>GS(on)</sub> = -10 V V <sub>DD</sub> = -30 V I <sub>b</sub> = -7 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 4.3 Ω
Rise Time	t <sub>r</sub>		110		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		160		ns	
Fall Time	t <sub>f</sub>		120		ns	
Total Gate Charge	Q <sub>G</sub>		42		nC	
Gate to Source Charge	Q <sub>GS</sub>		3		nC	V <sub>GS</sub> = -10 V I <sub>b</sub> = -16 A V <sub>DD</sub> = -48 V
Gate to Drain Charge	Q <sub>GD</sub>		17		nC	
Diode Forward Voltage	V <sub>SD</sub>		1.0		V	
Reverse Recovery Time	t <sub>rr</sub>		120		ns	I <sub>F</sub> = -14 A, V <sub>GS</sub> = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q <sub>rr</sub>		230		nC	

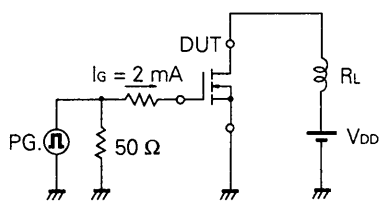
**Test Circuit 1 : Avalanche Capability**



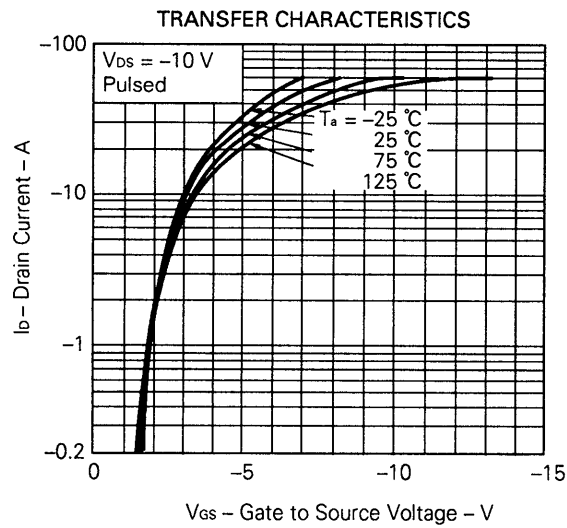
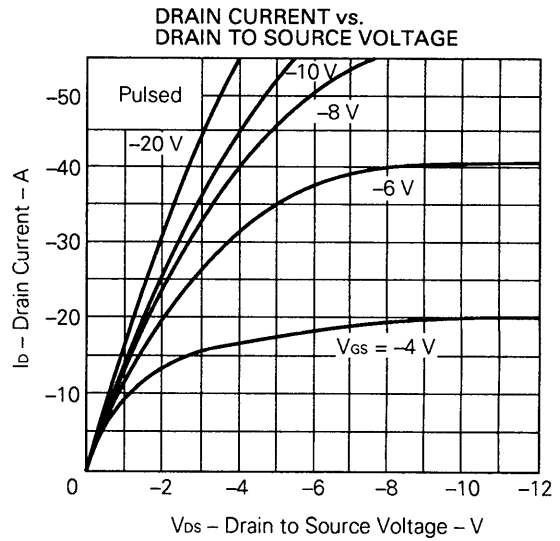
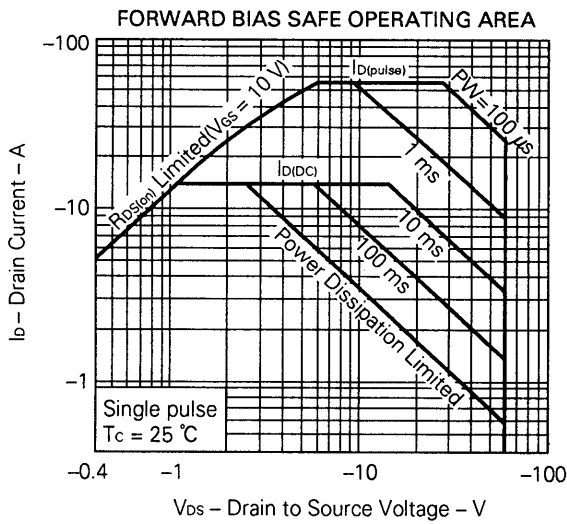
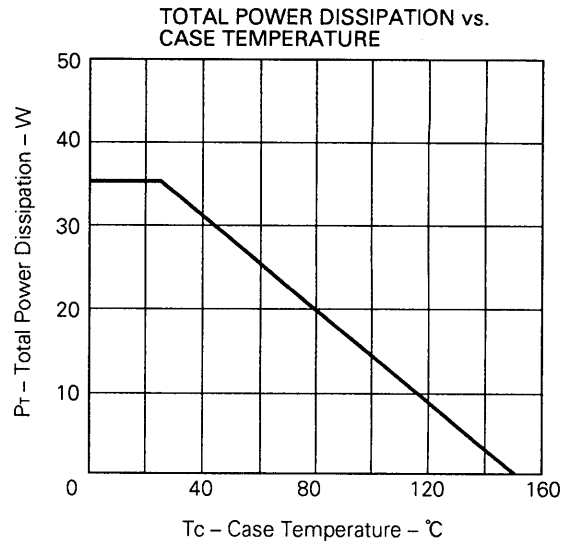
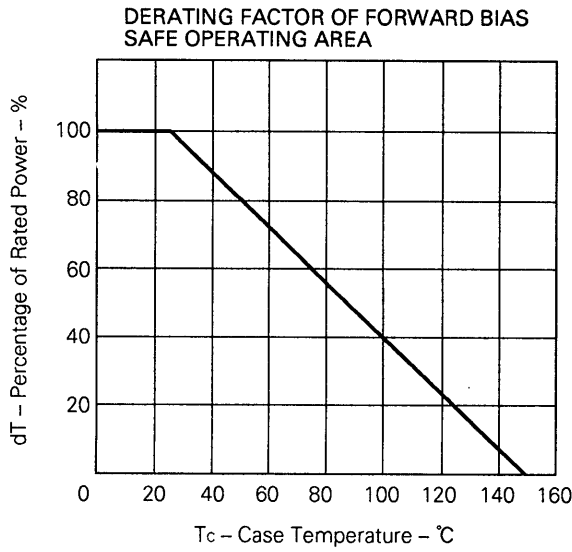
**Test Circuit 2 : Switching Time**

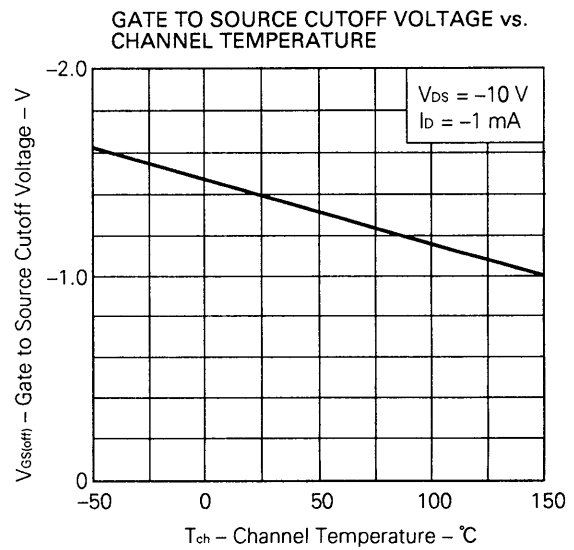
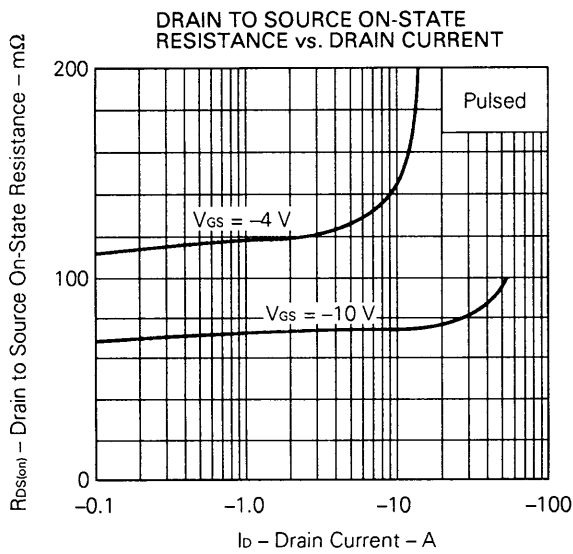
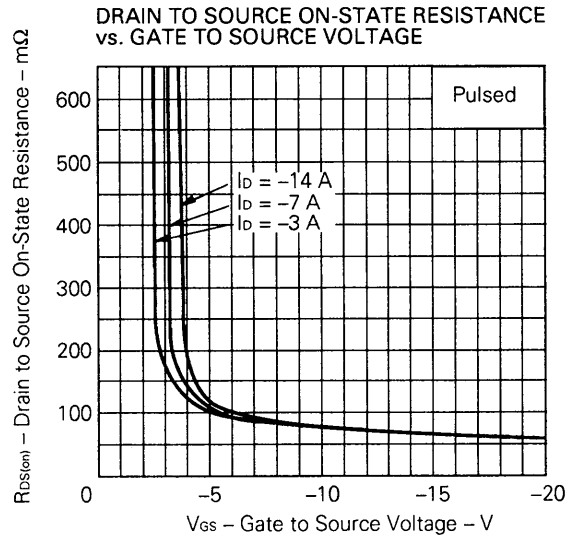
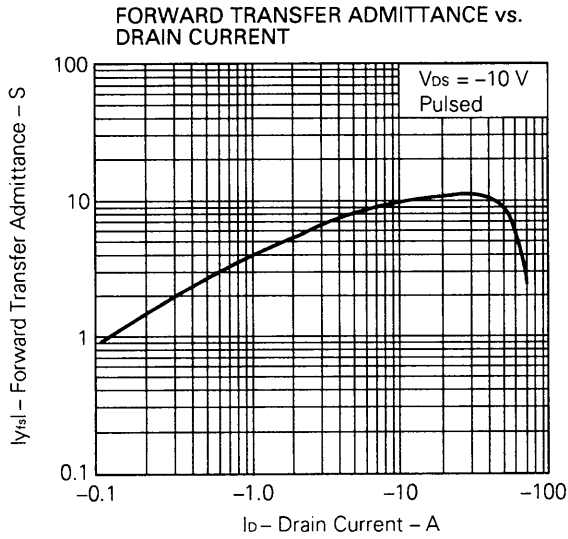
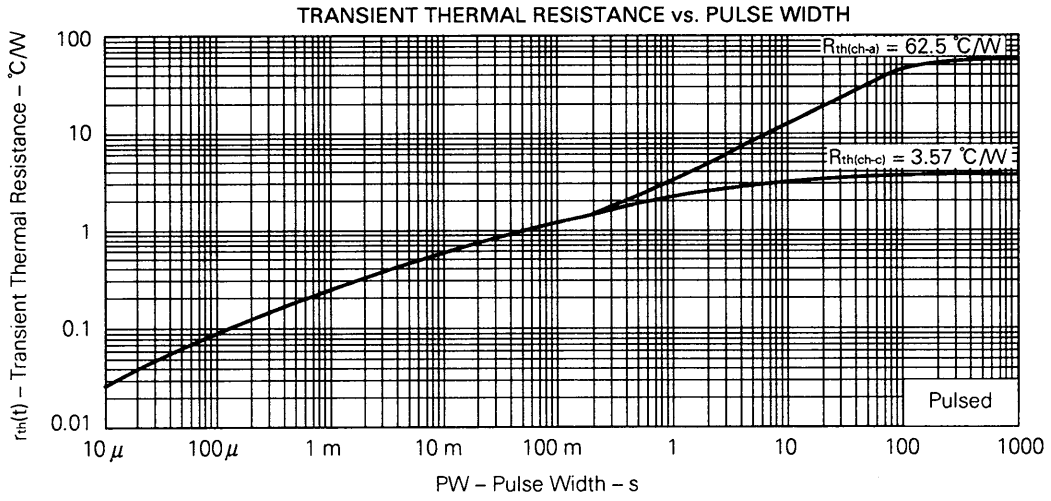


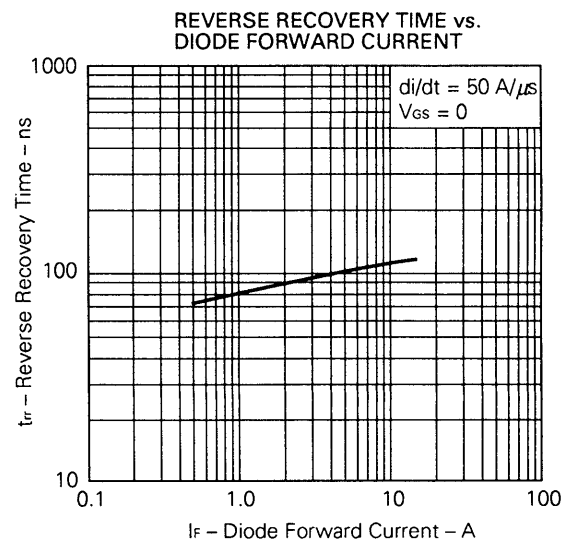
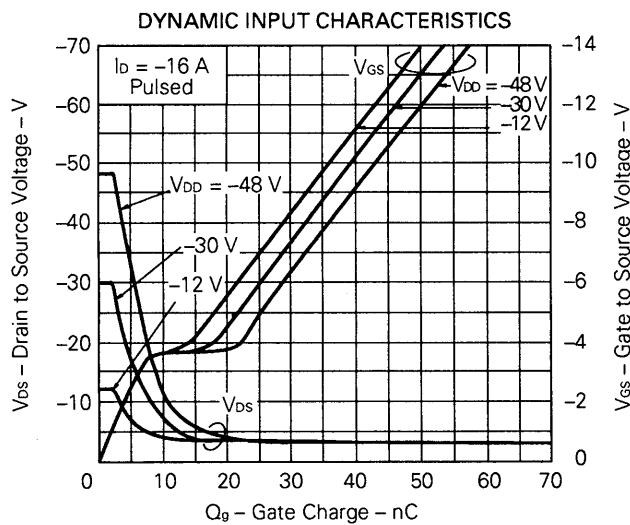
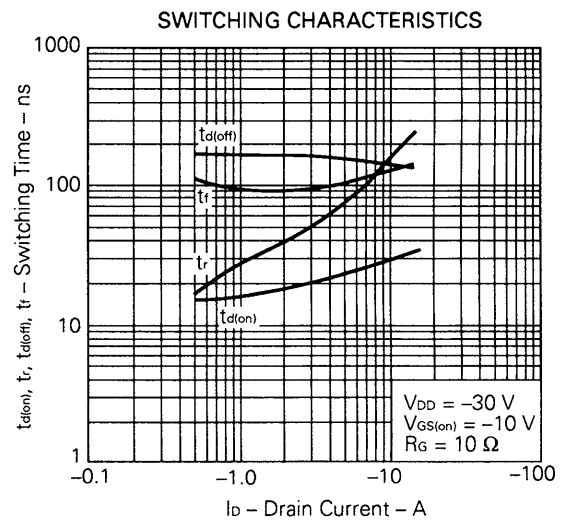
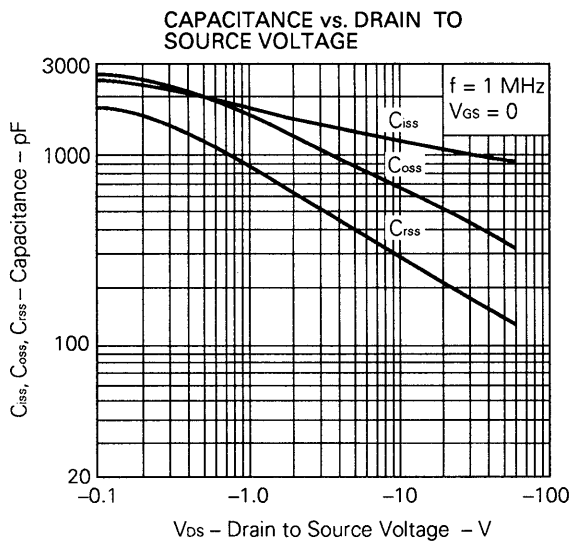
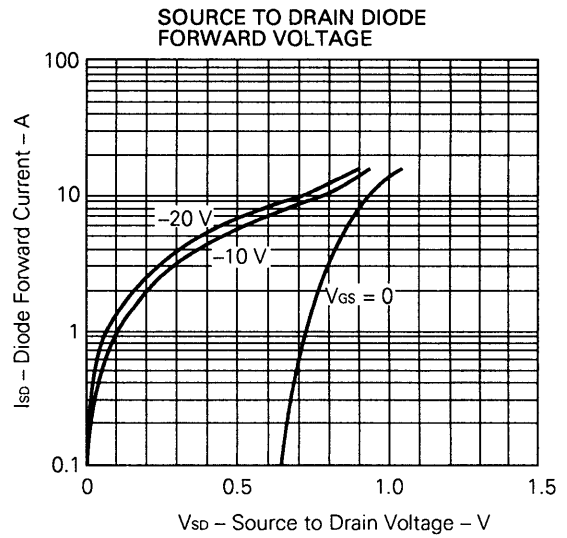
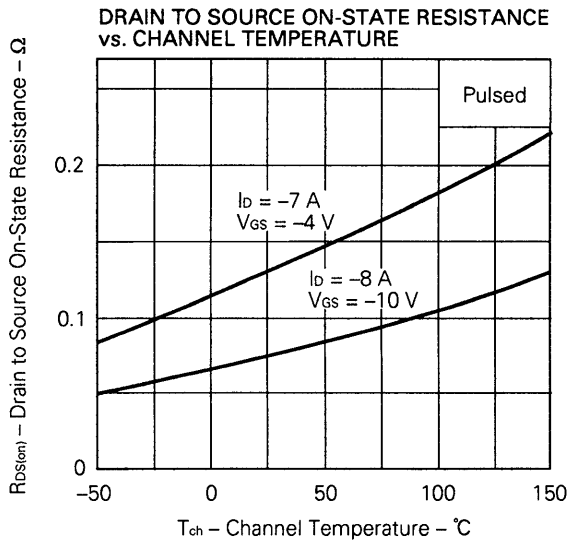
**Test Circuit 3 : Gate Charge**

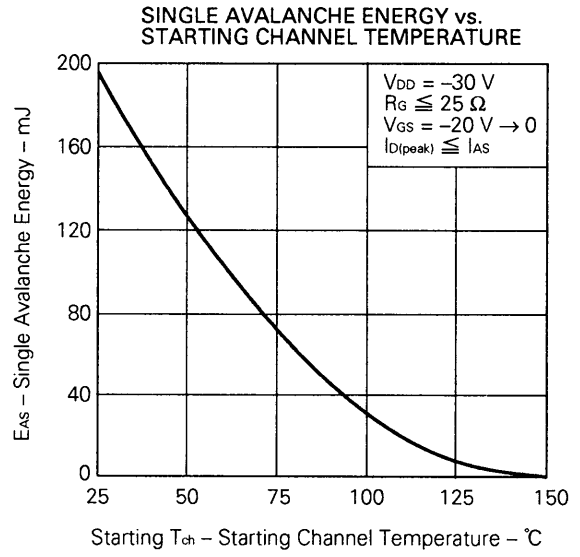
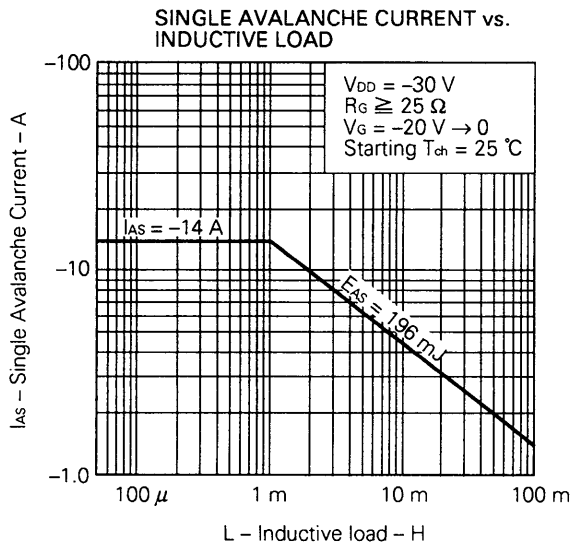


TYPICAL CHARACTERISTICS ( $T_a = 25\text{ }^\circ\text{C}$ )









**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207



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