NEC

MOS FIELD EFFECT TRANSISTOR

2SJ357

P-CHANNEL MOS FET FOR HIGH-SPEED SWITCH

The 2SJ357 is a P-channel vertical MOS FET that can be used as a switching element. The 2SJ357 can be directly driven by an IC operating at 5 V.

The 2SJ357 features a low on-resistance and excellent switching characteristics, and is suitable for applications such as actuator driver and DC/DC converter.

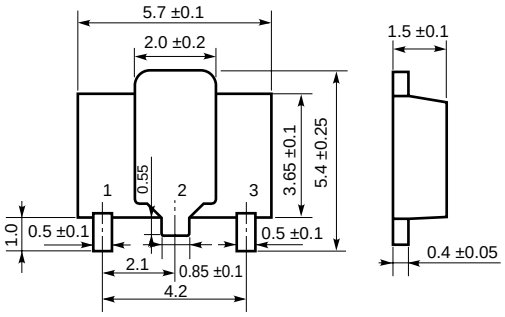
FEATURES

- New-type compact package
  Has advantages of packages for small signals and for power transistors, and compensates those disadvantages
- Can be directly driven by an IC operating at 5 V.
- Low on-resistance
  $R_{DS(ON)}$ = 0.35 Ω MAX. @V_{GS} = –4 V, I_D = –1.5 A
  $R_{DS(ON)}$ = 0.20 Ω MAX. @V_{GS} = –10 V, I_D = –1.5 A

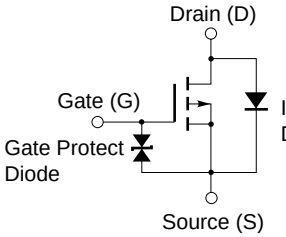
QUALITY GRADE

Standard

Package Drawings (unit: mm)



Equivalent Circuit



Electrode Connection
1. Source
2. Drain
3. Gate

Marking: UA1

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (T_A = +25 °C)

Parameter	Symbol	Conditions	Ratings	Unit
Drain-Source Voltage	V_{DSS}	V_{GS} = 0	–30	V
Gate-Source Voltage	V_{GSS}	V_{DS} = 0	–20/+10	V
Drain Current (DC)	$I_{D(DC)}$		–/+3.0	A
Drain Current (Pulse)	$I_{D(pulse)}$	PW ≤ 10 ms Duty Cycle ≤ 1 %	–/+6.0	A
Total Power Loss	P_T	Mounted on ceramic board of 7.5 cm^2 × 0.7 mm	2.0	W
Channel Temperature	T_{ch}		150	°C
Storage Temperature	T_{stg}		–55 to +150	°C

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

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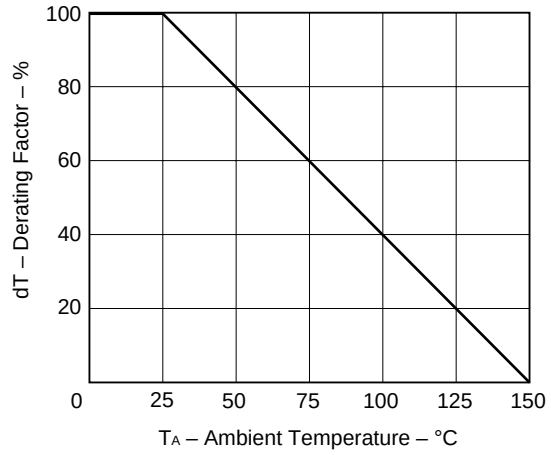
ELECTRICAL SPECIFICATIONS (T_A = +25 °C)

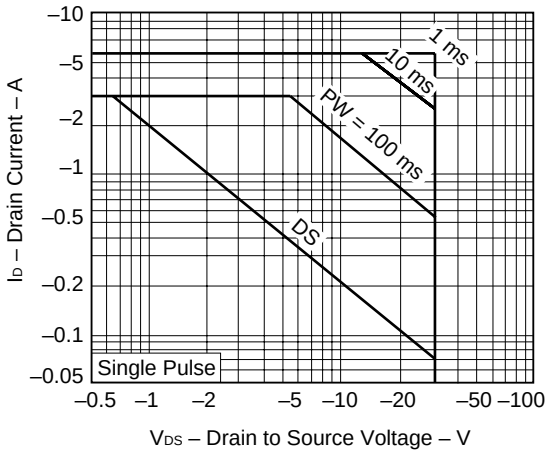
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Drain Shut-down Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0			–10	μA
Gate Leak Current	I_{GSS}	V_{GS} = –16/+10 V, V_{DS} = 0			–/+10	μA
Gate Cutoff Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0	–1.5	–2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –1.0 A	1.8			S
Drain-Source On-Resistance	$R_{DS(on)1}$	V_{GS} = –4 V, I_D = –1.5 A		0.23	0.35	Ω
Drain-Source On-Resistance	$R_{DS(on)2}$	V_{GS} = –10 V, I_D = –1.5 A		0.12	0.20	Ω
Input Capacitance	C_{iss}	V_{DS} = –10 V, V_{GS} = 0, f = 1.0 MHz		645		pF
Output Capacitance	C_{oss}			500		pF
Feedback Capacitance	C_{rss}			275		pF
On-Time Delay	$t_{d(on)}$	V_{DD} = –25 V, I_D = –1.5 A, $V_{GS(on)}$ = –10 V, R_G = 10 Ω, R_L = 17 Ω		8		ns
Rise Time	t_r			42		ns
Off-Time Delay	$t_{d(off)}$			145		ns
Fall Time	t_f			170		ns
Gate Input Charge	Q_G	V_{DS} = –24 V, V_{GS} = –10 V, I_D = –3.1 A, I_G = –2 mA		25.1		nC
Gate-Source Chanrge	Q_{GS}			2.0		nC
Gate-Drain Charge	Q_{GD}			9.8		nC
Internal Diode Reverse Recovery Time	t_{rr}	I_F = 3.0 A, di/dt = 50 A/μs		112		ns
Internal Diode Reverse Recovery Charge	Q_{rr}			106		nC

CHARACTERISTICS CURVES (T_A = +25 °C)

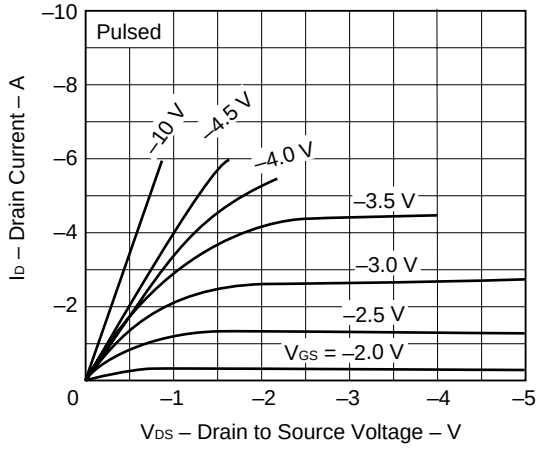
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



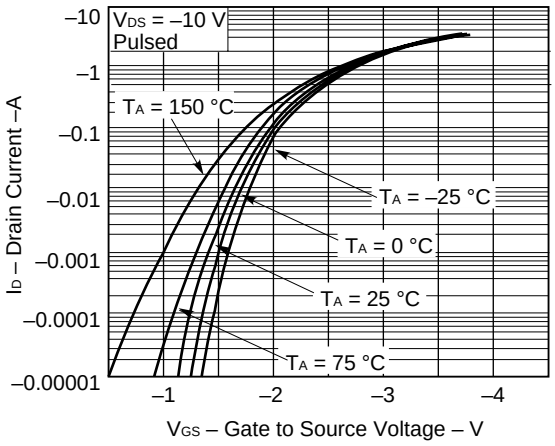
FORWARD BIAS SAFE OPERATING AREA



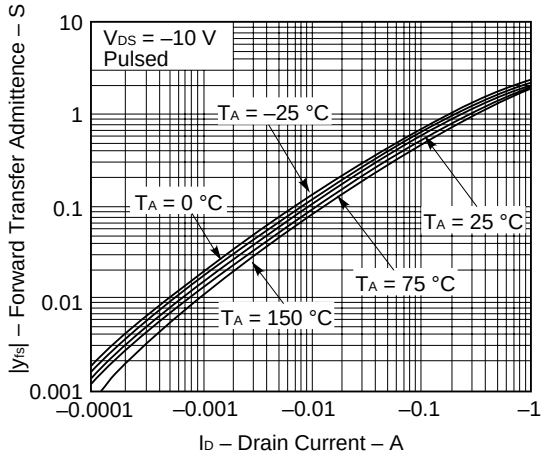
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



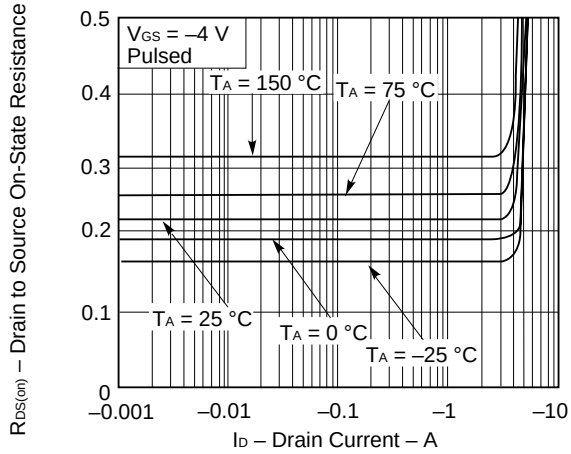
TRANSFER CHARACTERISTICS



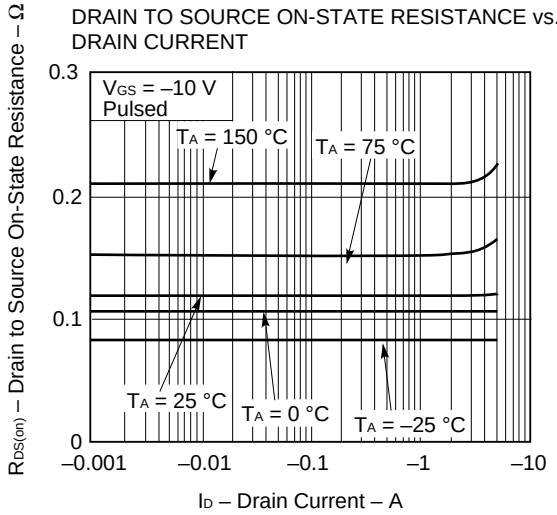
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



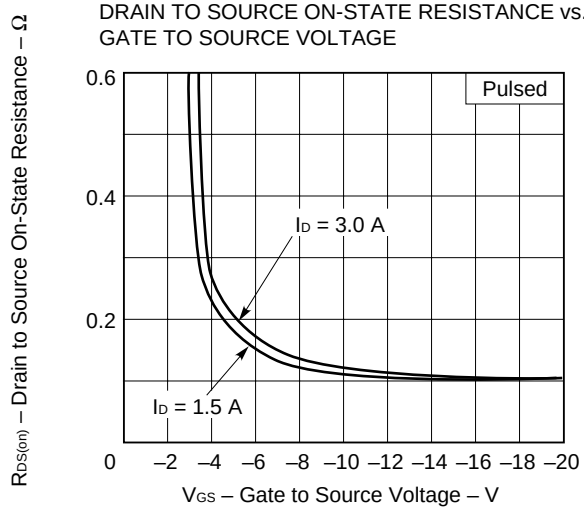
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRINT



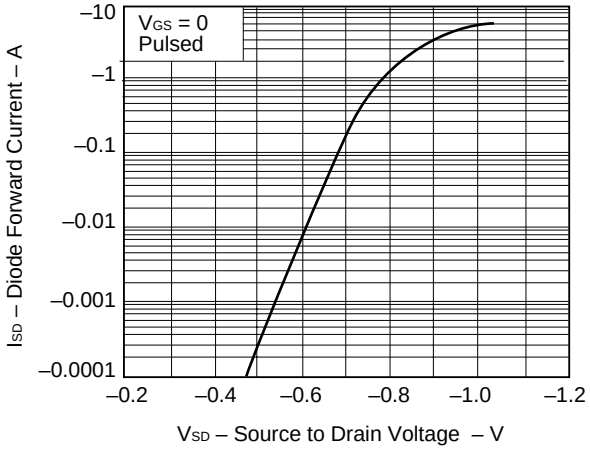
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



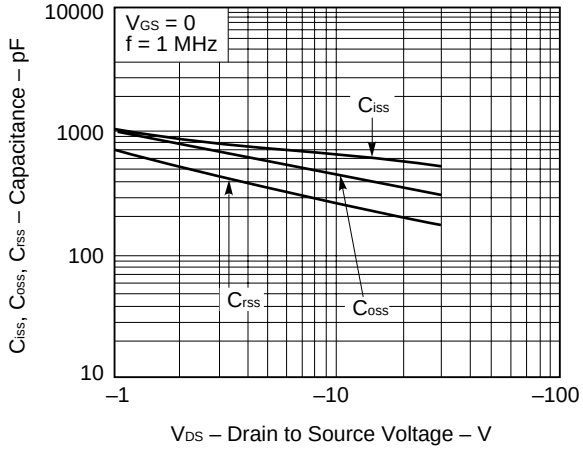
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



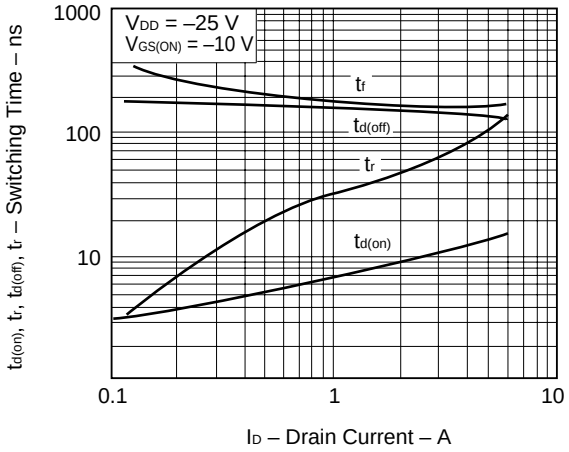
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



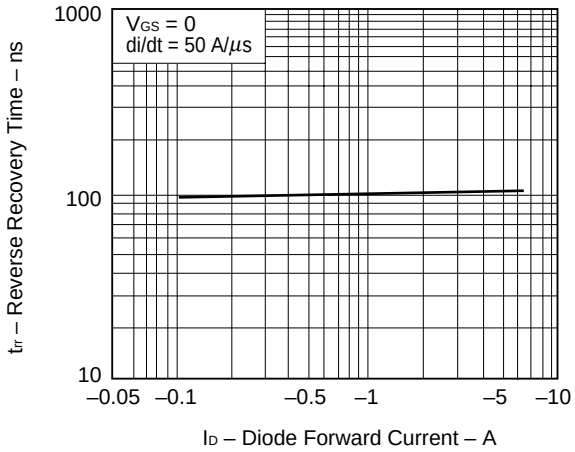
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



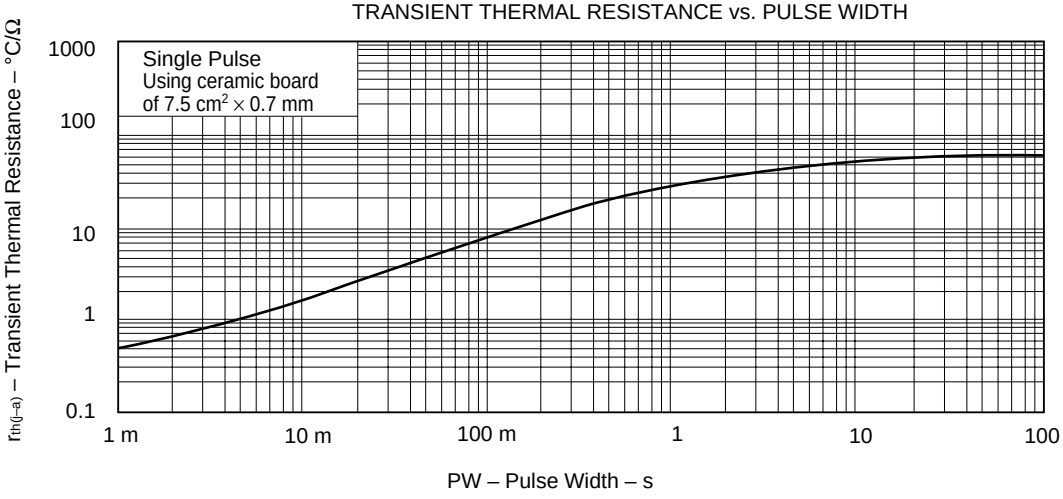
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



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