MOS FIELD EFFECT POWER TRANSISTORS

SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

This product is P-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super Low On-State Resistance $R_{DS(on)1} = 30 \text{ m}\Omega \text{ MAX}. (V_{GS} = -10 \text{ V}, I_D = -15 \text{ A})$ $R_{DS(on)2} = 56 \text{ m}\Omega \text{ MAX}. (V_{GS} = -4 \text{ V}, I_D = -15 \text{ A})$
- Low Ciss Ciss = 4120 pF TYP.

EC

Built-in Gate Protection Diode

ABSOLUTE MAXIMUM RATINGS (TA = 25° C)

Drain to Source Voltage	Vdss	-60	V
Gate to Source Voltage*	VGSS(AC)	∓20	V
Gate to Source Voltage	VGSS(DC)	-20, 0	V
Drain Current (DC)	ID(DC)	∓30	А
Drain Current (pulse)**	D(pulse)	∓120	А
Total Power Dissipation (Tc = 25°C)	Pτ	35	W
Total Power Dissipation ($T_A = 25^{\circ}C$)	Pτ	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
*f = 20 kHz, Duty Cycle \leq 10% (+Side)			



2SJ495

THERMAL RESISTANCE

**PW \leq 10 μ s, Duty Cycle \leq 1%

Channel	to	Case
Channel	to	Ambient

Rth(ch-c)	3.57	°C/W
Rth(ch-A)	62.5	°C/W

MP-45F (ISOLATED TO-220)



The diode connected between the gate and source of the transistor serves as a protector against ESD. When this deveice acutally used, an additional protection circiut is externally required if a voltage exceeding the rated voltage may be applied to this device.

ELECTRICAL	CHARACTERISTICS	(T _A = 25°C)
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CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	$V_{GS} = -10 V, I_D = -15 A$		24	30	mΩ
	RDS(on)2	$V_{GS} = -4 V$, $I_D = -15 A$		38	56	mΩ
Gate to Source Cutoff Voltage	VGS(off)	$V_{DS} = -10 \text{ V}, \text{ I}_{D} = -1 \text{ mA}$	-1.0	-1.5	-2.0	V
Forward Transfer Admittance	y _{fs}	$V_{DS} = -10 V, I_{D} = -15 A$	12	24		S
Drain Leakage Current	Ibss	$V_{DS} = -60 V, V_{GS} = 0$			-10	μA
Gate to Source Leakage Current	Igss	$V_{GS} = \mp 20 \text{ V}, \text{ V}_{DS} = 0$			∓10	μA
Input Capacitance	Ciss	Vds = -10 V		4120		pF
Output Capacitance	Coss	Vgs = 0		1750		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		580		pF
Turn-On Delay Time	td(on)	I⊳ = −15 A		40		ns
Rise Time	tr	$V_{GS(on)} = -10 V$		220		ns
Turn-Off Delay Time	td(off)	$V_{DD} = -30 V$		600		ns
Fall Time	tr	Rg = 10 Ω		380		ns
Total Gate Charge	QG	ID = -30 A		140		nC
Gate to Source Charge	QGS	$V_{DD} = -48 V$		12		nC
Gate to Drain Charge	QGD	$V_{GS} = -10 V$		46		nC
Body Diode Forward Voltage	VF(S-D)	IF = 30 A, VGS = 0		0.8	1.5	V
Reverse Recovery Time	trr	IF = 30 A, VGS = 0		160		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ μ s		400		nC

Test Circuit 1 Switching Time



Test Circuit 2 Gate Charge



t = 1 μ s Duty Cycle \leq 1%



FORWARD BIAS SAFE OPERATING AREA



FORWARD TRANSFER CHARACTERISTICS











FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT





DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE







CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE





SWITCHING CHARACTERISTICS





Document Name	Document No.		
NEC semicondacter device reliability/quality control system	C11745E		
Power MOS FET features and application to switching power supply	D12971E		
Application circuits using Power MOS FET	TEA-1035		
Safe operating area of Power MOS FET	TEA-1037		
Guide to prevent damage for semiconductor devices by electrostatic discharge (EDS)	C11892E		

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- Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
- Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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Anti-radioactive design is not implemented in this product.