Ordering number:EN4112

N-Channel Junction Silicon FET

2SK1740

HF amplifiers low frequency amplifiers analog switches

Features

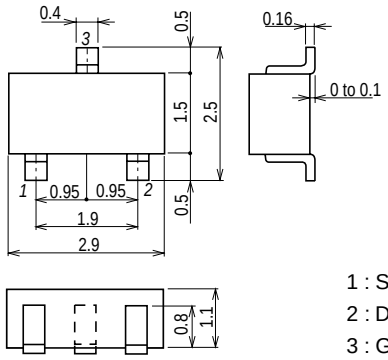
- Adoption of FBET process.
- Large $|y_{fs}|$.
- Small Ciss.
- Small-sized package permitting 2SK1740-applied sets to be made small and slim.

Package Dimensions

unit:mm

2050A

[2SK1740]



1 : Source
2 : Drain
3 : Gate
SANYO : CP

Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSX}		40	V
Gate-to-Drain Voltage	V_{GDS}		–40	V
Gate Current	I_G		10	mA
Drain Current	I_D		75	mA
Allowable Power Dissipation	P_D		250	mW
Junction Temperature	Tj		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C

Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Gate-to-Drain Breakdown Voltage	$V_{(BR)GDS}$	I_G=–10μA, V_{DS}=0	–40			V
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=–20V, V_{DS}=0V			–1.0	nA
Cutoff Voltage	$V_{GS(off)}$	V_{DS}=10V, I_D=100μA	–2.0	–3.0	–5.0	V
Zero-Gate Voltage Drain Current	I_{DSS}*	V_{DS}=10V, V_{GS}=0V	40*		75*	mA
Forward Transfer Admittance	| yfs |1	V_{DS}=10V, I_D=10mA, f=1kHz	10	15		mS
	| yfs |2	V_{DS}=10V, V_{GS}=0V, f=1kHz	22	30		mS

* : Pulse Test Pulse Width ≤ 2ms

Continued on next page.

* : The 2SK1740 is classified by I_{DSS} as follows (unit : mA) :

40	3	52	48	4	63	57	5	75

Marking : IJ

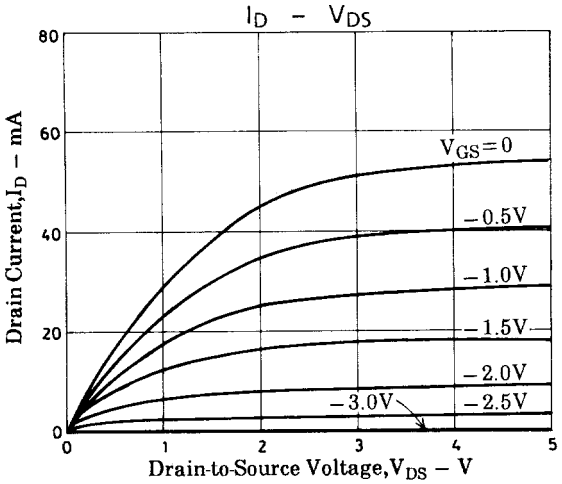
I_{DSS} rank : 3, 4, 5

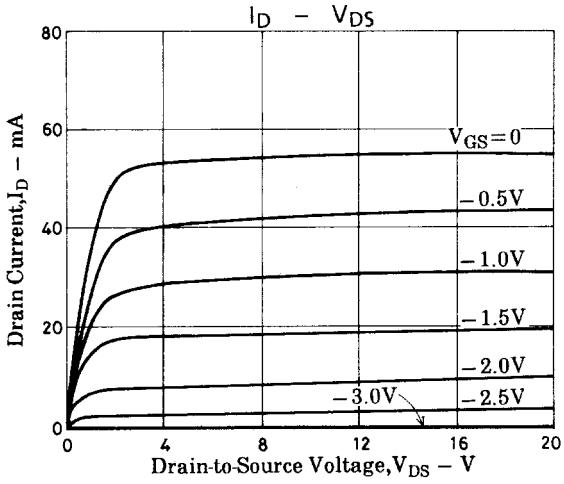
SANYO Electric Co.,Ltd. Semiconductor Company

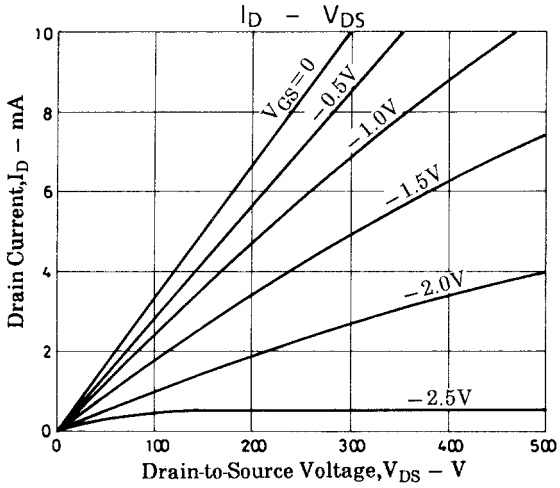
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

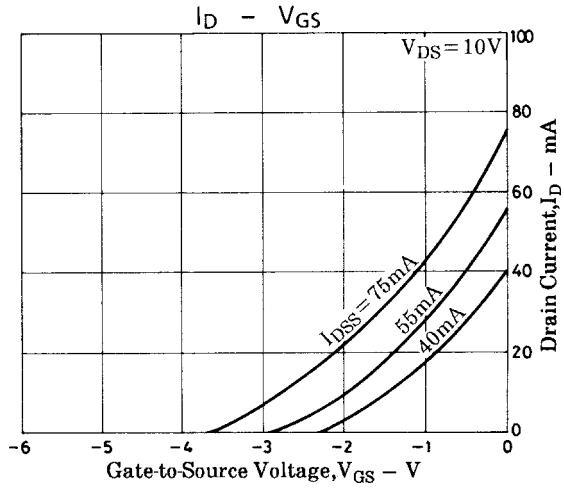
Continued from preceding page.

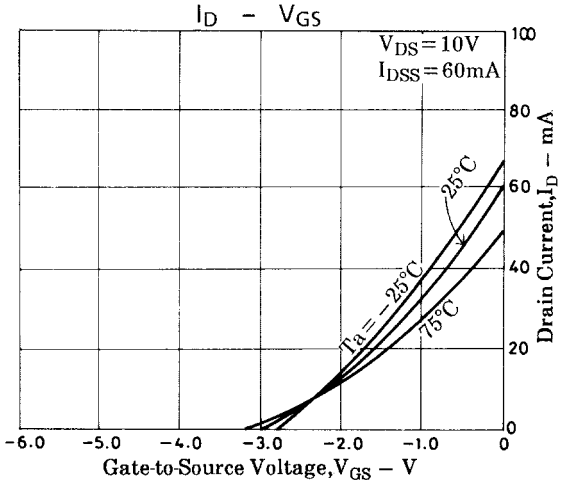
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input Capacitance	Ciss	V_{DS}=10V, V_{GS}=0V, f=1MHz		11		pF
Reverse Transfer Capacitance	Crss	V_{DS}=10V, V_{GS}=0V, f=1MHz		2.5		pF
Noise Figure	NF	V_{DS}=10V, Rg=1kΩ, I_D=1mA, f=1kHz		1.5		dB
Static Drain-to-Source on State Resistance	$R_{DS(on)}$	I_D=10mA, V_{GS}=0		30		Ω

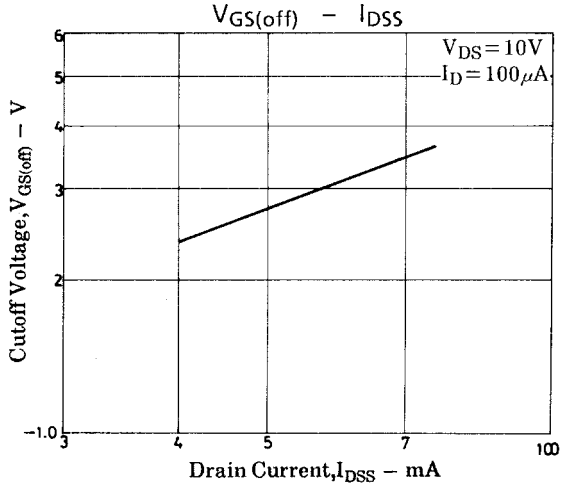




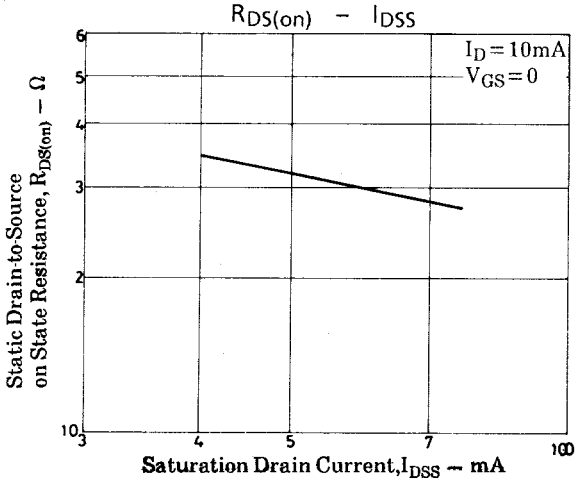




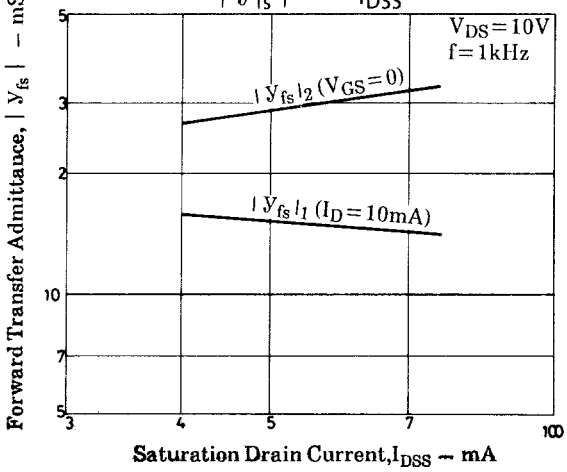




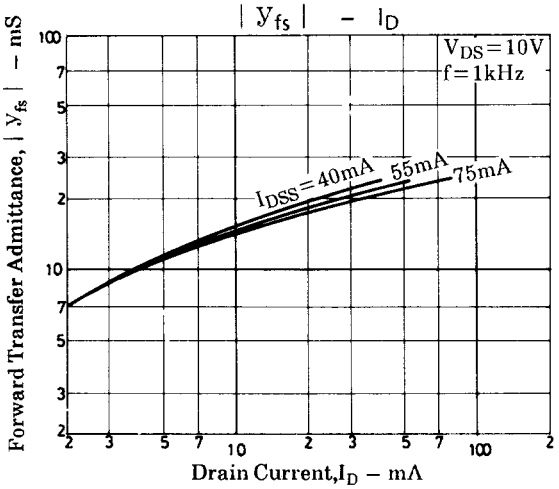
$R_{DS(on)}$ – I_{DSS}



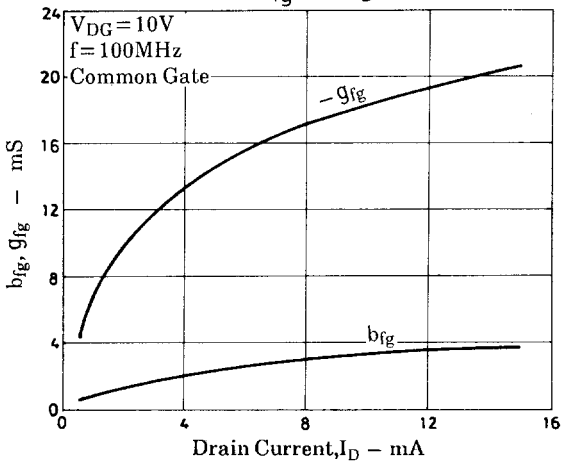
$|y_{fs}|$ – I_{DSS}



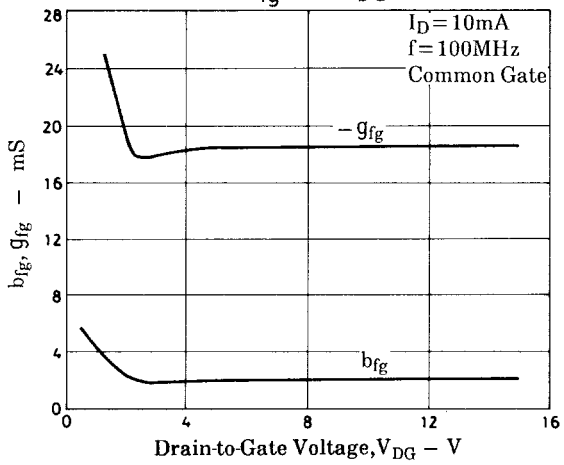
$|y_{fs}|$ – I_D



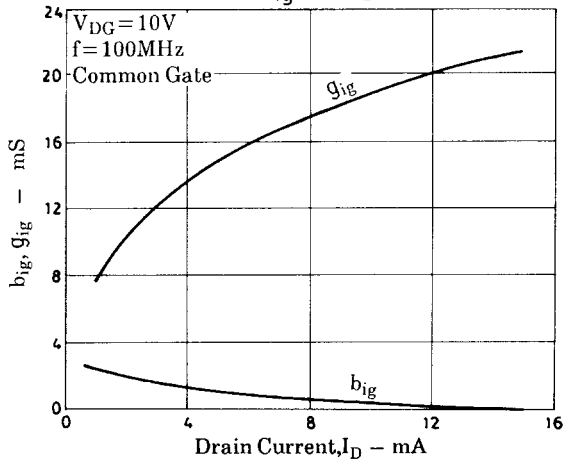
y_{fg} – I_D



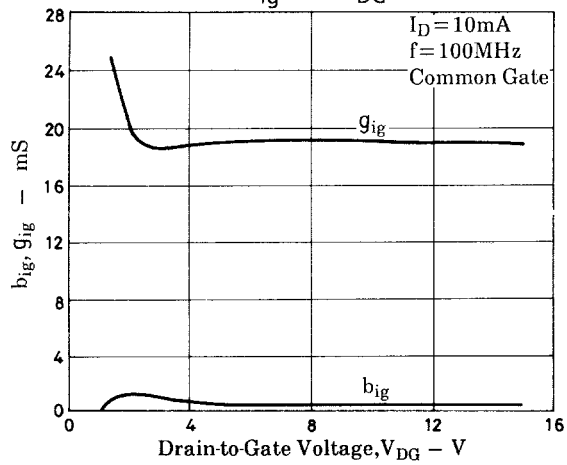
y_{fg} – V_{DG}



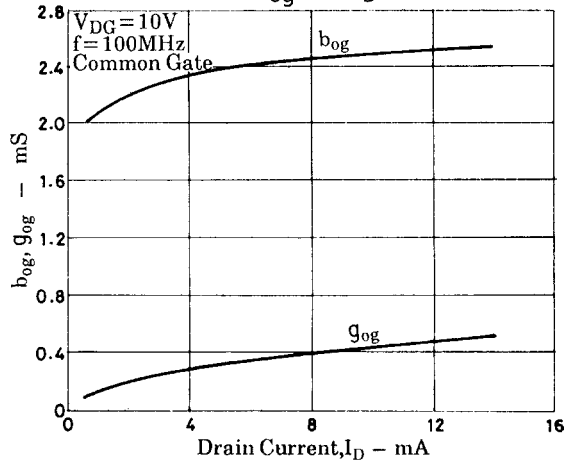
y_{ig} – I_D

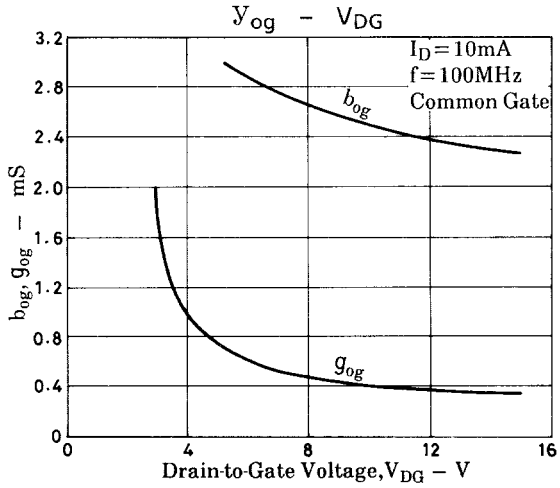


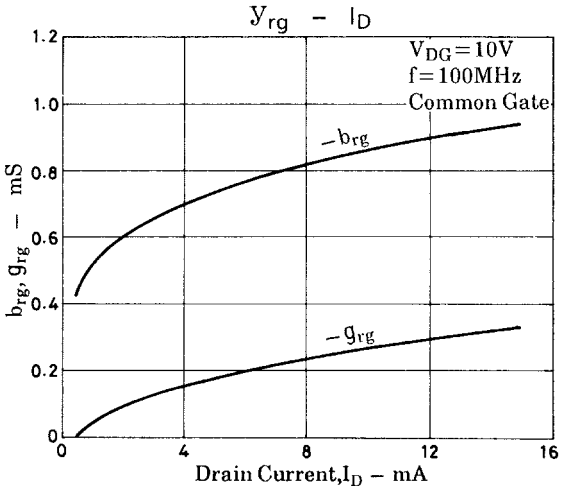
y_{ig} – V_{DG}

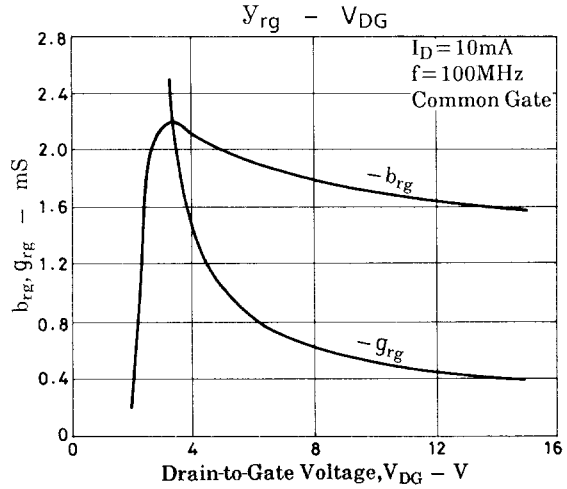


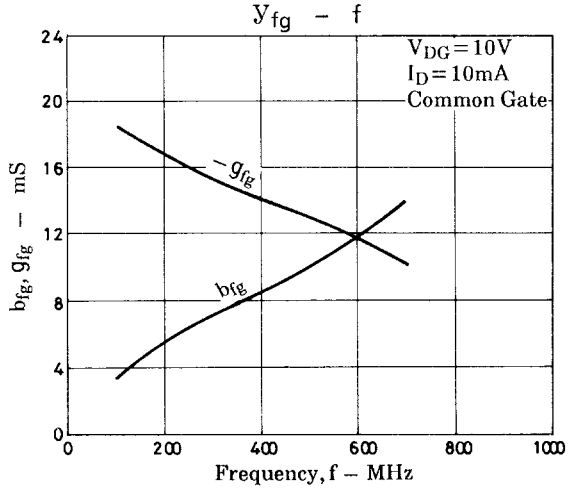
y_{og} – I_D

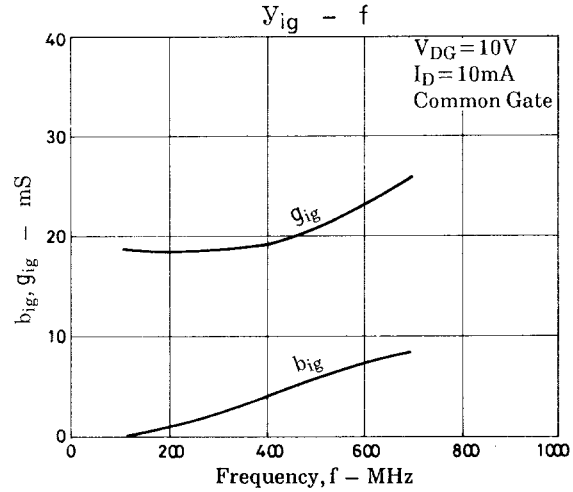


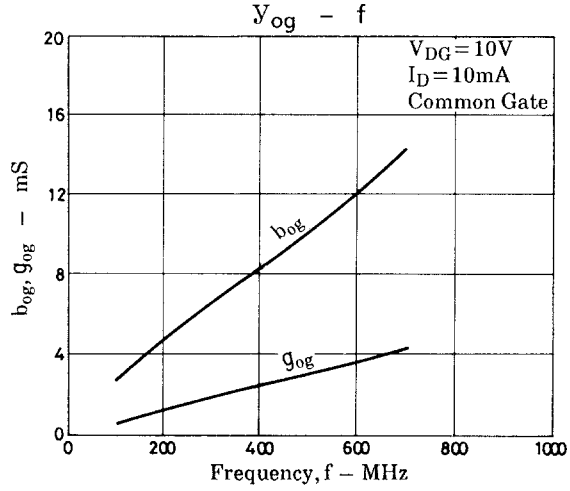

y_{og} – V_{DG}
I_D=10mA
f=100MHz
Common Gate
b_{og}
g_{og}
b_{og}, g_{og} – mS
Drain-to-Gate Voltage, V_{DG} – V

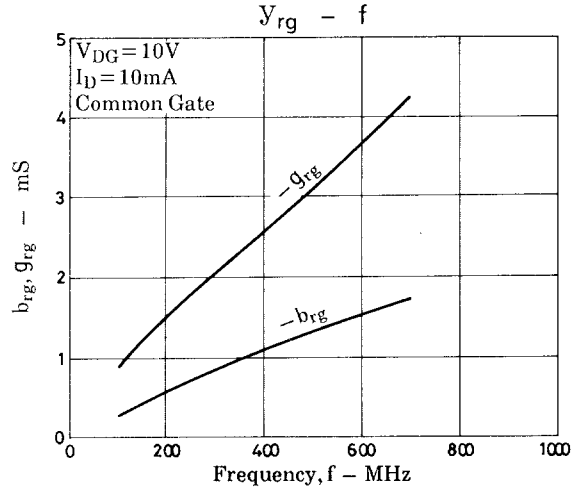

y_{rg} – I_D
V_{DG}=10V
f=100MHz
Common Gate
$-b_{rg}$
$-g_{rg}$
b_{rg}, g_{rg} – mS
Drain Current, I_D – mA

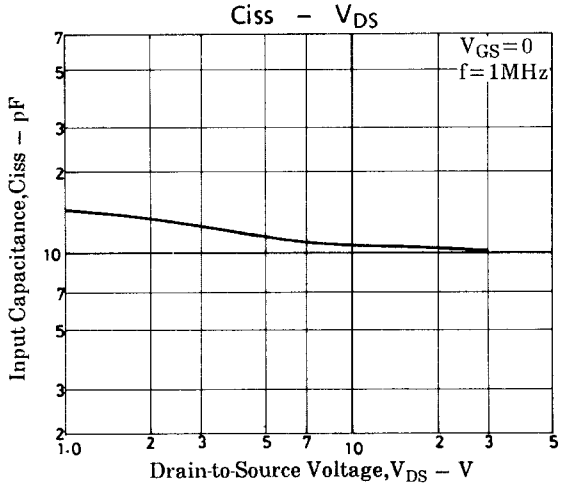

y_{rg} – V_{DG}
I_D=10mA
f=100MHz
Common Gate
$-b_{rg}$
$-g_{rg}$
b_{rg}, g_{rg} – mS
Drain-to-Gate Voltage, V_{DG} – V


y_{fg} – f
V_{DG}=10V
I_D=10mA
Common Gate
$-g_{fg}$
b_{fg}
b_{fg}, g_{fg} – mS
Frequency, f – MHz


y_{ig} – f
V_{DG}=10V
I_D=10mA
Common Gate
g_{ig}
b_{ig}
b_{ig}, g_{ig} – mS
Frequency, f – MHz


y_{og} – f
V_{DG}=10V
I_D=10mA
Common Gate
b_{og}
g_{og}
b_{og}, g_{og} – mS
Frequency, f – MHz


y_{rg} – f
V_{DG}=10V
I_D=10mA
Common Gate
$-g_{rg}$
$-b_{rg}$
b_{rg}, g_{rg} – mS
Frequency, f – MHz


Ciss – V_{DS}
V_{GS}=0
f=1MHz
Input Capacitance, Ciss – pF
Drain-to-Source Voltage, V_{DS} – V