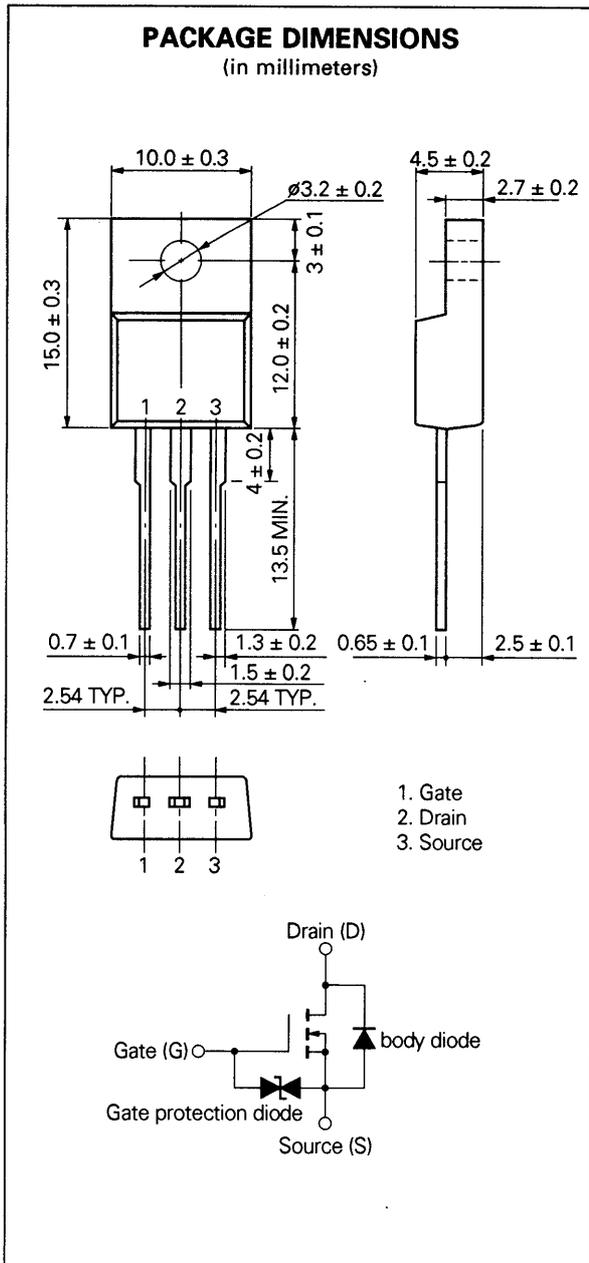


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P1 98.2

MOS FIELD EFFECT POWER TRANSISTOR 2SK2234

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE



DESCRIPTION

The 2SK2234 is N-channel Power MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 0.6 \Omega$ MAX. ($V_{GS} = 10 V$, $I_D = 4.0 A$)
- Low C_{iss} $C_{iss} = 1\ 500$ pF TYP.
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

| | | |
|---------------------|-------------|---------|
| Storage Temperature | -55 to +150 | °C |
| Channel Temperature | 150 | °C MAX. |

Maximum Power Dissipation

| | | |
|--|-----|---|
| Total Power Dissipation ($T_c = 25$ °C) | 40 | W |
| Total Power Dissipation ($T_a = 25$ °C) | 2.0 | W |

Maximum Voltages and Currents ($T_a = 25$ °C)

| | | | |
|-----------------|-------------------------|------|---|
| V_{DSS} | Drain to Source Voltage | 500 | V |
| V_{GSS} | Gate to Source Voltage | ±30 | V |
| $I_{D(DC)}$ | Drain Current (DC) | ±8.0 | A |
| $I_{D(pulse)*}$ | Drain Current (pulse) | ±32 | A |

Maximum Avalanche Capability Ratings**

| | | | |
|----------|--------------------------|-----|----|
| I_{AS} | Single Avalanche Current | 12 | A |
| E_{AS} | Single Avalanche Energy | 362 | mJ |

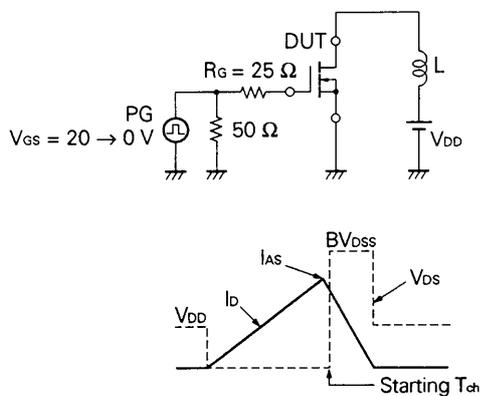
* $PW \leq 10 \mu s$, Duty Cycle $\leq 1\%$

** Starting $T_{ch} = 25$ °C, $R_G = 25 \Omega$, $V_{GS} = 20 V \rightarrow 0$

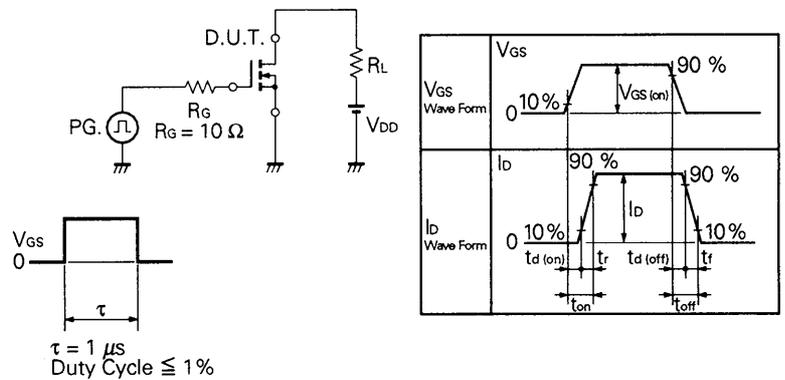
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|-------------------------------------|----------------------|------|-------|------|------|---|
| Drain to Source On-state Resistance | R _{DS(on)} | | 0.5 | 0.6 | Ω | V _{GS} = 10 V, I _D = 4 A |
| Gate to Source Cutoff Voltage | V _{GS(off)} | 2.5 | | 3.5 | V | V _{DS} = 10 V, I _D = 1 mA |
| Forward Transfer Admittance | y _{fs} | 3.0 | | | S | V _{DS} = 10 V, I _D = 4 A |
| Drain Leakage Current | I _{DSS} | | | 100 | μA | V _{DS} = 500 V, V _{GS} = 0 |
| Gate to Source Leakage Current | I _{GSS} | | | ±10 | μA | V _{GS} = ±20 V, V _{DS} = 0 |
| Input Capacitance | C _{iss} | | 1 500 | | pF | V _{DS} = 10 V V _{GS} = 0 f = 1 MHz |
| Output Capacitance | C _{oss} | | 480 | | pF | |
| Reverse Transfer Capacitance | C _{res} | | 200 | | pF | |
| Turn-On Delay Time | t _{d(on)} | | 23 | | ns | V _{GS} = 10 V V _{DD} = 150 V I _D = 4 A, R _G = 10 Ω R _L = 37.5 Ω |
| Rise Time | t _r | | 23 | | ns | |
| Turn-Off Delay Time | t _{d(off)} | | 104 | | ns | |
| Fall Time | t _f | | 21 | | ns | |
| Total Gate Charge | Q _G | | 57 | | nC | V _{GS} = 10 V I _D = 8 A V _{DD} = 400 V |
| Gate to Source Charge | Q _{GS} | | 8.6 | | nC | |
| Gate to Drain Charge | Q _{GD} | | 3.4 | | nC | |
| Diode Forward Voltage | V _{F(S-D)} | | 1.0 | | V | I _F = 8 A, V _{GS} = 0 |
| Reverse Recovery Time | t _{rr} | | 435 | | ns | I _F = 8 A di/dt = 50 A/μs |
| Reverse Recovery Charge | Q _{rr} | | 2.1 | | μC | |

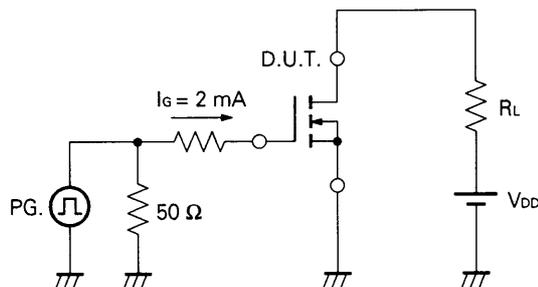
Test Circuit 1: Avalanche Capability



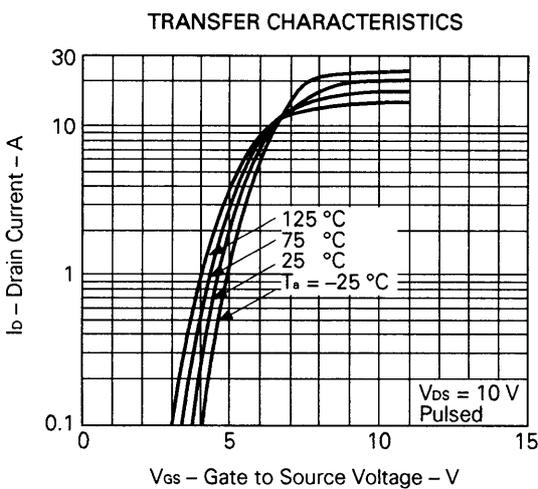
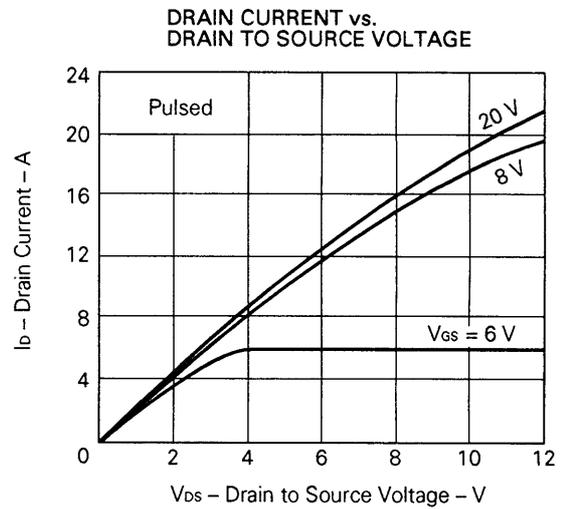
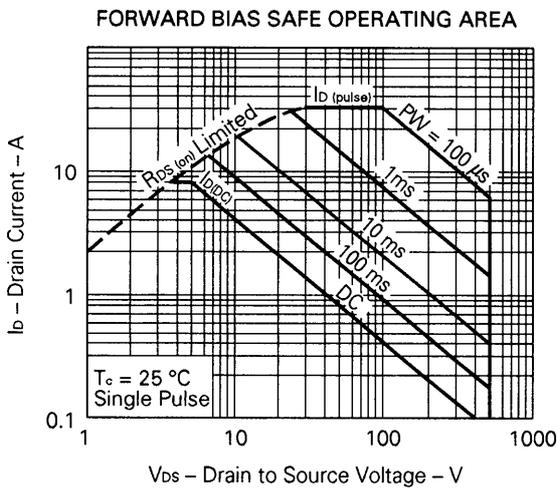
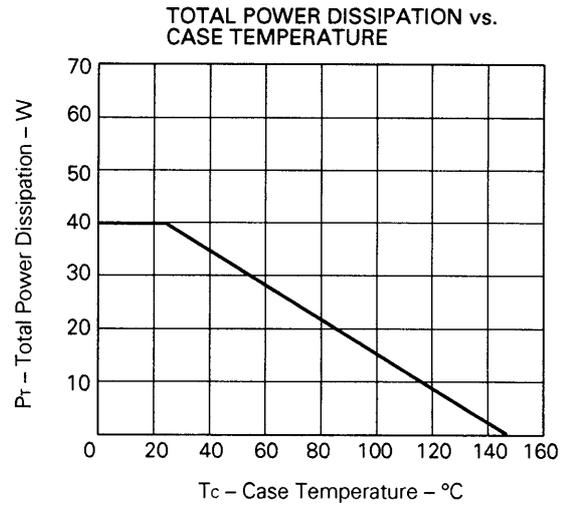
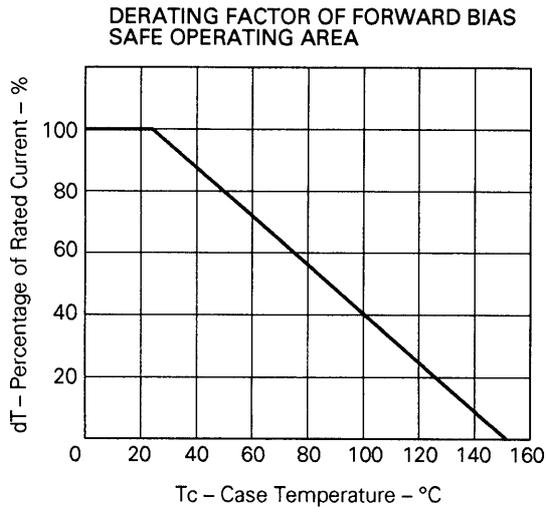
Test Circuit 2: Switching Time



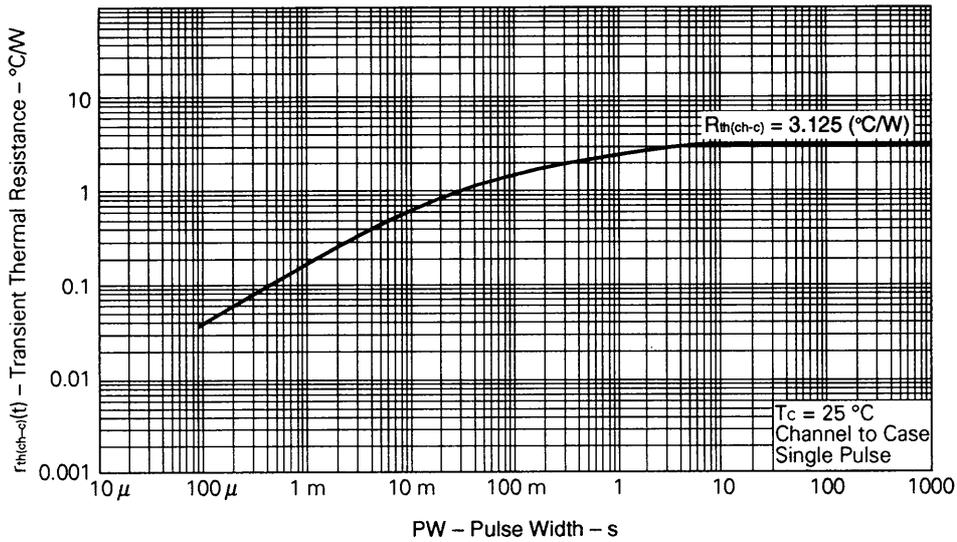
Test Circuit 3: Gate Charge



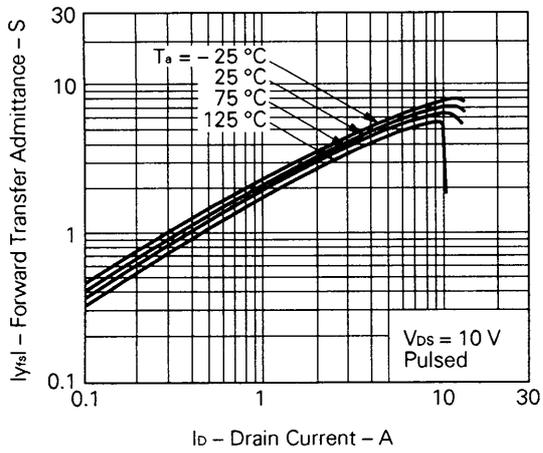
TYPICAL CHARACTERISTICS ($T_a = 25\text{ }^\circ\text{C}$)



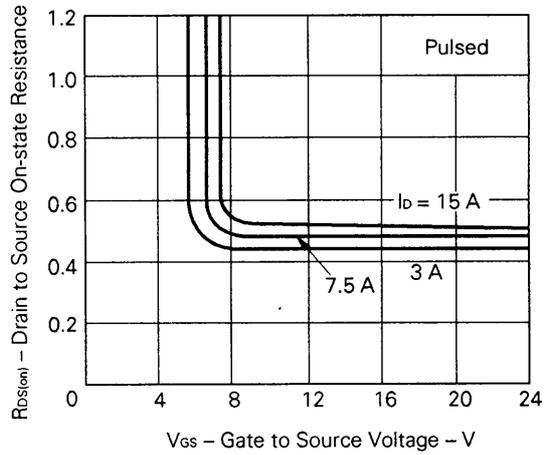
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



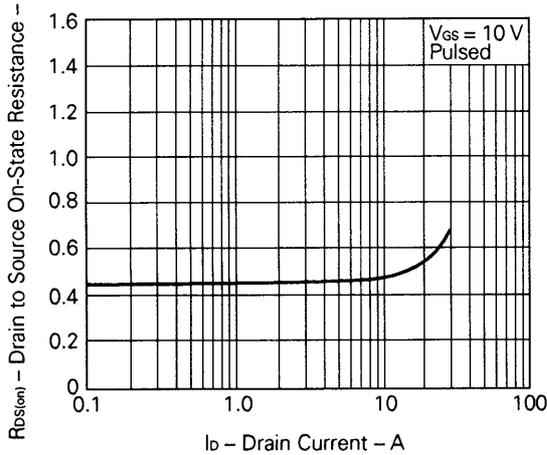
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



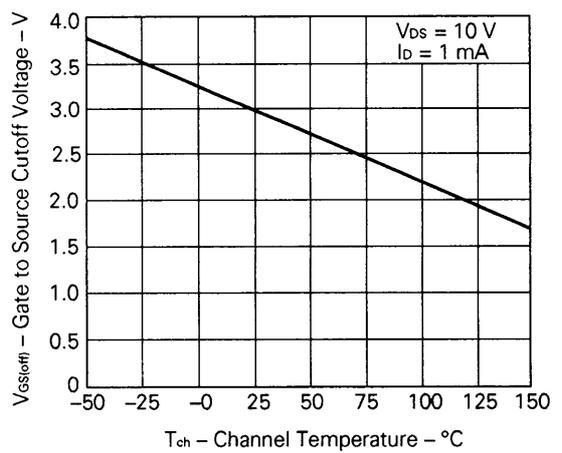
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



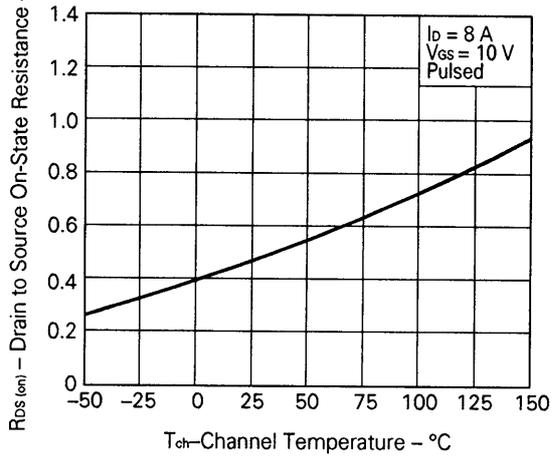
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



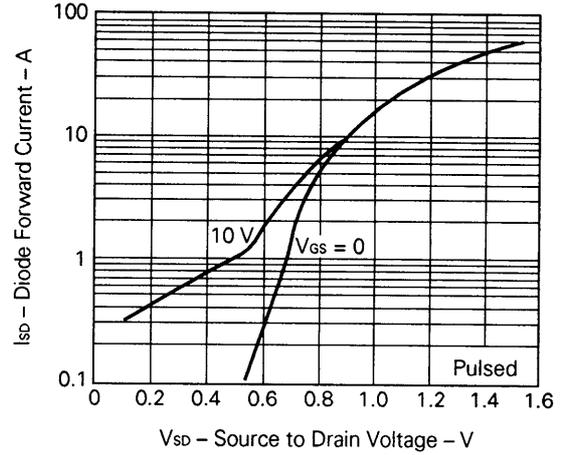
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



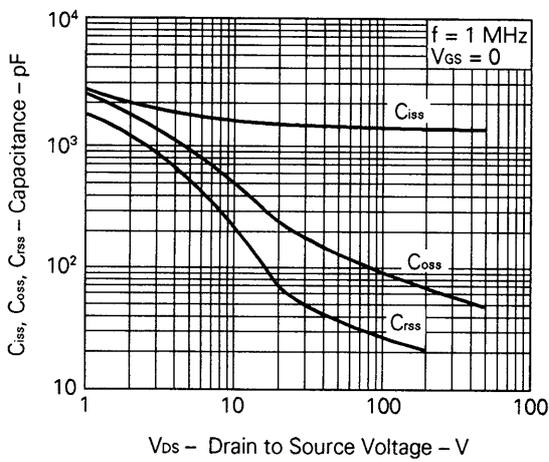
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



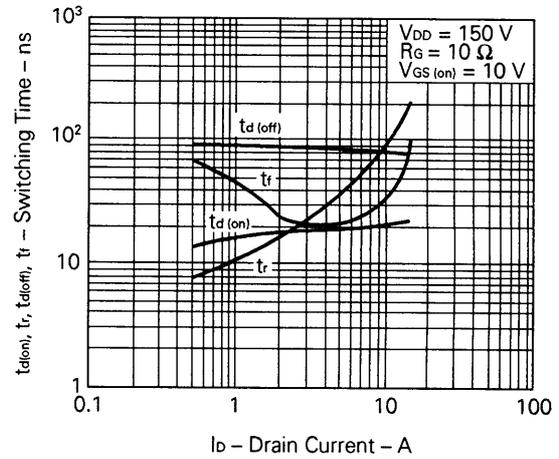
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



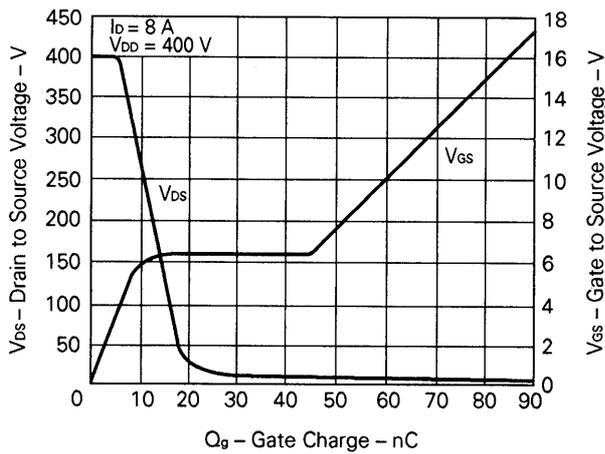
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



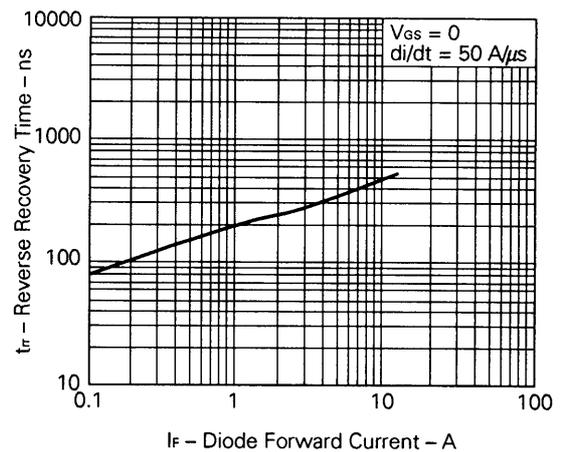
SWITCHING CHARACTERISTICS

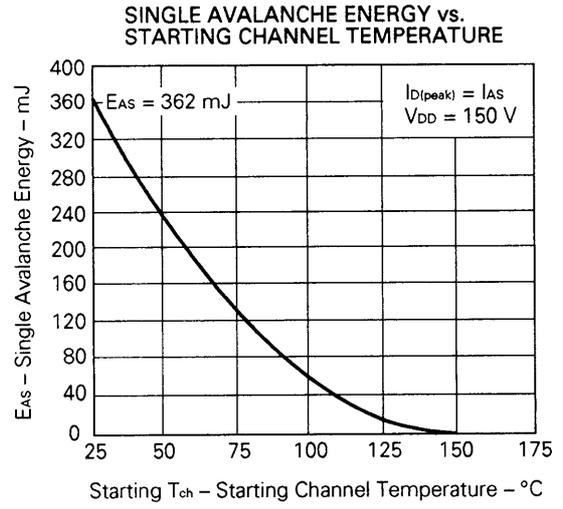
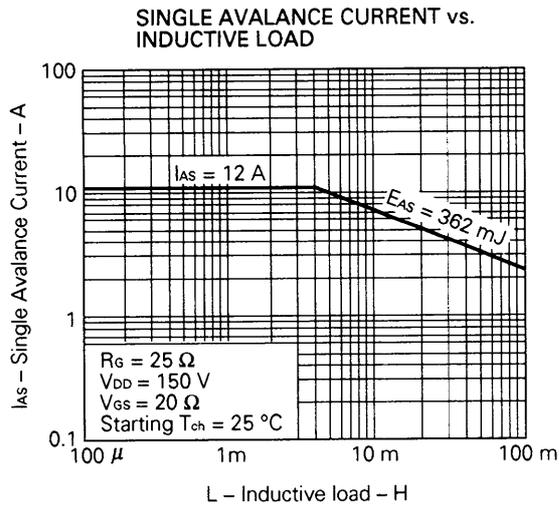


DYNAMIC INPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT





Reference

| Application note name | No. |
|--|----------|
| Safe operating area of Power MOS FET. | TEA-1034 |
| Application circuit using Power MOS FET. | TEA-1035 |
| Quality control of NEC semiconductors devices. | TEI-1202 |
| Quality control guide of semiconductors devices. | MEI-1202 |
| Assembly manual of semiconductors devices. | IEI-1207 |

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