

MOS FIELD EFFECT TRANSISTOR **2SK2414, 2SK2414-Z**

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK2414 is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

Low On-Resistance

 $\begin{array}{l} {\sf R}_{\sf DS(on)1} = 70 \ {\sf m}\Omega \ {\sf M}{\sf AX}. \ (@ \ {\sf V}_{\sf GS} = 10 \ {\sf V}, \ {\sf I}_{\sf D} = 5.0 \ {\sf A}) \\ {\sf R}_{\sf DS(on)2} = 95 \ {\sf m}\Omega \ {\sf M}{\sf AX}. \ (@ \ {\sf V}_{\sf GS} = 4 \ {\sf V}, \ {\sf I}_{\sf D} = 5.0 \ {\sf A}) \end{array}$

- Low C_{iss} C_{iss} = 840 pF TYP.
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (TA = 25 $^{\circ}$ C)

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Drain to Source Voltage	Vdss	60	V
Gate to Source Voltage	Vgss	±20	V
Drain Current (DC)	D(DC)	±10	А
Drain Current (pulse)*	D(pulse)	±40	А
Total Power Dissipation (Tc = 25 °C)	P _{T1}	20	W
Total Power Dissipation (T _A = 25 °C)	Рт2	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current**	las	10	А
Single Avalanche Energy**	Eas	10	mJ

* PW \leq 10 μ s, Duty Cycle \leq 1 %

** Starting T_{ch} = 25 °C, R_G = 25 Ω , V_{GS} = 20 V \rightarrow 0



The information in this document is subject to change without notice.

ELECTRICAL CHARACTERISTICS (TA = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	RDS(on)1		52	70	mΩ	Vgs = 10 V, Id = 5.0 A
Drain to Source On-Resistance	RDS(on)2		68	95	mΩ	Vgs = 4 V, Id = 5.0 A
Gate to Source Cutoff Voltage	VGS(off)	1.0	1.6	2.0	V	$V_{DS} = 10 V, I_D = 1 mA$
Forward Transfer Admittance	y _{fs}	7.0	12		S	V _{DS} = 10 V, I _D = 5.0 A
Drain Leakage Current	Idss			10	μA	$V_{DS} = 60 V, V_{GS} = 0$
Gate to Source Leakage Current	lgss			±10	μA	$V_{GS} = \pm 20 \text{ V}, \text{ V}_{DS} = 0$
Input Capacitance	Ciss		860		pF	V _{DS} = 10 V
Output Capacitance	Coss		440		pF	V _{GS} = 0
Reverse Transfer Capacitance	Crss		110		pF	f = 1 MHz
Turn-On Delay Time	td(on)		15		ns	ID = 5.0 A
Rise Time	tr		90		ns	$V_{GS(on)} = 10 V$
Turn-Off Delay Time	td(off)		75		ns	V _{DD} = 30 V
Fall Time	tr		35		ns	R _G = 10 Ω
Total Gate Charge	QG		24		nC	ID = 10 A
Gate to Source Charge	QGS		2.6		nC	V _{DD} = 48 V
Gate to Drain Charge	Qgd		6.0		nC	Vgs = 10 V
Body Diode Forward Voltage	VF(S-D)		1.0		V	IF = 10 A, VGS = 0
Reverse Recovery Time	trr		85		ns	IF = 10 A, VGS = 0
Reverse Recovery Charge	Qrr		220		nC	di/dt = 50 A/µs

Test Circuit 1 Avalanche Capability

Test Circuit 2 Switching Time







Test Circuit 3 Gate Charge



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

TYPICAL CHARACTERISTICS (TA = 25 $^{\circ}$ C)





FORWARD BIAS SAFE OPERATING AREA



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE





FORWARD TRANSFER CHARACTERISTICS



PW - Pulse Width - s





DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE











REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	C11745E
Quality grade on NEC semiconductor devices.	C11531E
Semiconductor device mounting technology manual.	C10535E
IC package manual.	C10943X
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	X10679E
Power MOS FET features and application switching power supply.	D12971E
Application circuits using Power MOS FET.	D12972E
Safe operating area of Power MOS FET.	D13085E

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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Anti-radioactive design is not implemented in this product.

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