

MOS FIELD EFFECT TRANSISTOR
2SK2478

**SWITCHING
 N-CHANNEL POWER MOS FET
 INDUSTRIAL USE**

DESCRIPTION

The 2SK2478 is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-Resistance
 $R_{DS(on)} = 7.5 \Omega$ ($V_{GS} = 10 V, I_D = 1.0 A$)
- Low C_{iss} $C_{iss} = 485 pF$ TYP.
- High Avalanche Capability Ratings
- Isolated TO-220 Package

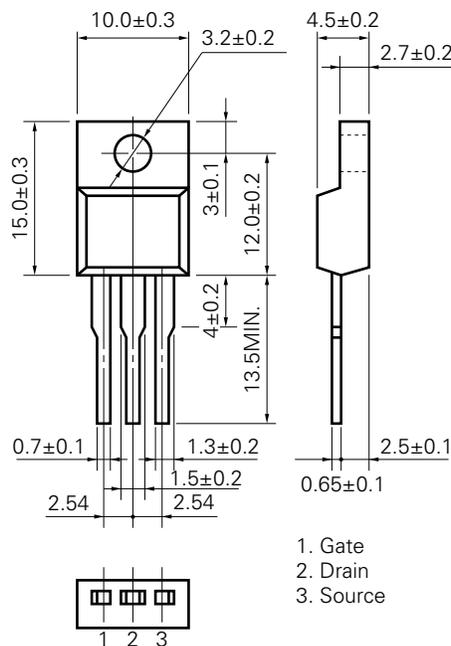
ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ }^\circ\text{C}$)

Drain to Source Voltage	V_{DS}	900	V
Gate to Source Voltage	V_{GS}	± 30	V
Drain Current (DC)	$I_{D(DC)}$	± 2.0	A
Drain Current (pulse)*	$I_{D(pulse)}$	± 8.0	A
Total Power Dissipation ($T_c = 25 \text{ }^\circ\text{C}$)	P_{T1}	30	W
Total Power Dissipation ($T_A = 25 \text{ }^\circ\text{C}$)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current**	I_{AS}	2.0	A
Single Avalanche Energy**	E_{AS}	16.5	mJ

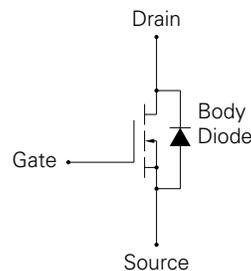
* PW - 10 μs , Duty Cycle - 1 %

** Starting $T_{ch} = 25 \text{ }^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 V \rightarrow 0$

**PACKAGE DIMENSIONS
 (in millimeter)**



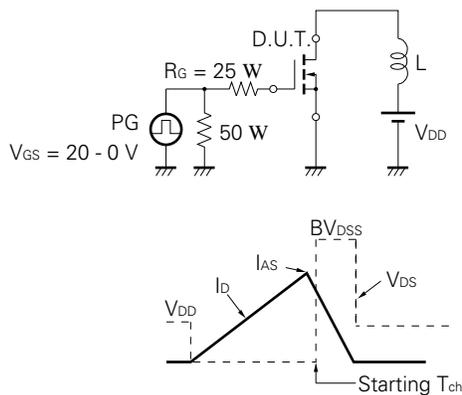
MP-45F (ISOLATED TO-220)



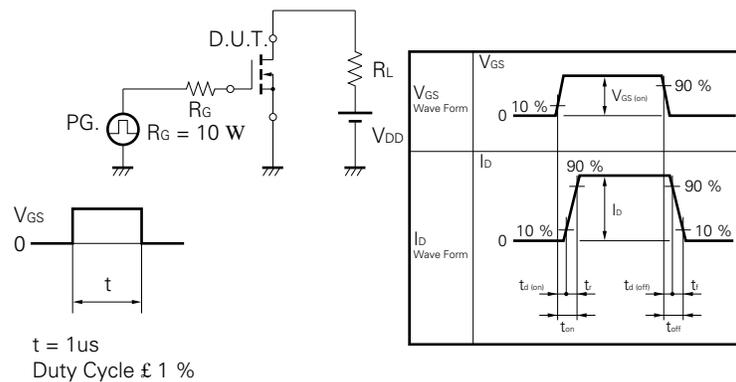
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	R _{DS(on)}		5.0	7.5	Ω	V _{GS} = 10 V, I _D = 1.0 A
Gate to Source Cutoff Voltage	V _{GS(off)}	2.5		3.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	0.6			S	V _{DS} = 20 V, I _D = 1.0 A
Drain Leakage Current	I _{DSS}			100	μA	V _{DS} = V _{DSS} , V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±100	nA	V _{GS} = ±30 V, V _{DS} = 0
Input Capacitance	C _{iss}		485		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		75		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		10		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		11		ns	I _D = 1.0 A
Rise Time	t _r		3		ns	V _{GS} = 10 V
Turn-Off Delay Time	t _{d(off)}		35		ns	V _{DD} = 150 V
Fall Time	t _f		8		ns	R _G = 150 Ω
Total Gate Charge	Q _G		17		nC	I _D = 2.0 A
Gate to Source Charge	Q _{GS}		3		nC	V _{DD} = 450 V
Gate to Drain Charge	Q _{GD}		8		nC	V _{GS} = 10 V
Body Diode Forward Voltage	V _{F(S-D)}		1.0		V	I _F = 2.0 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		580		ns	I _F = 2.0 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		2.3		μC	di/dt = 50 A/μs

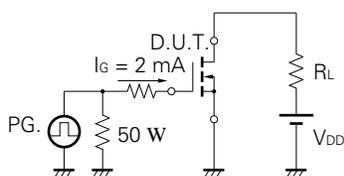
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time

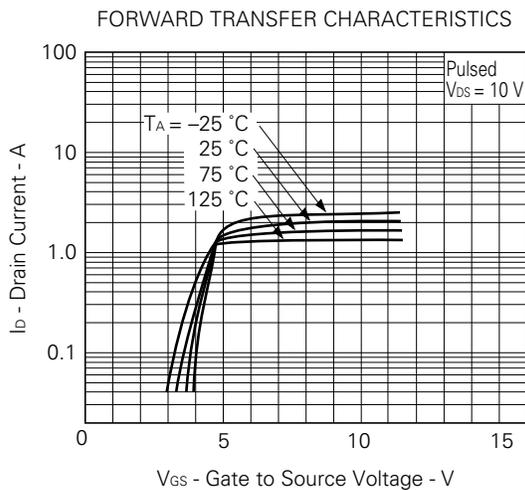
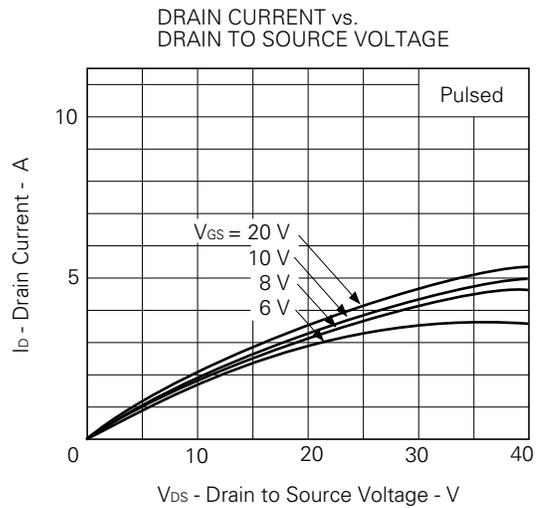
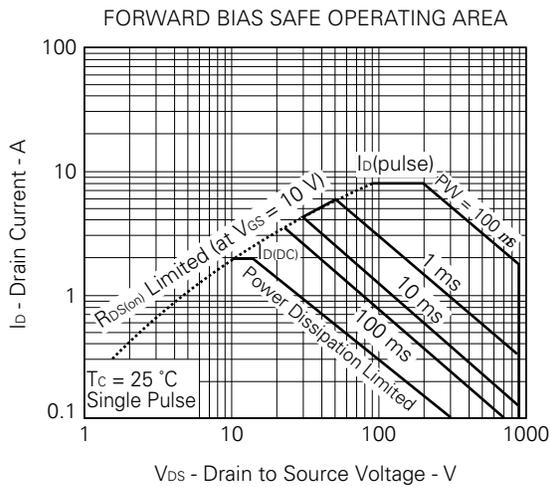
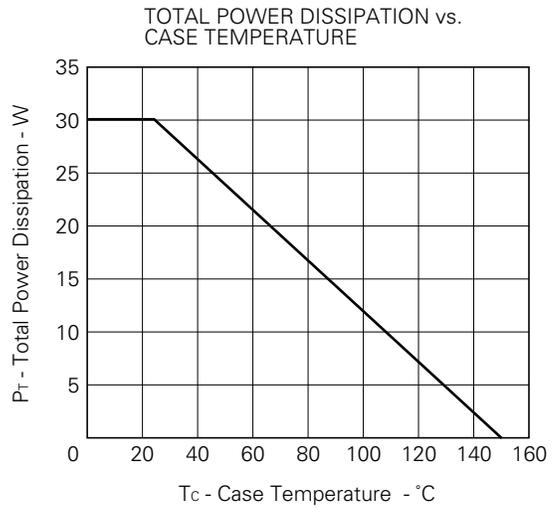
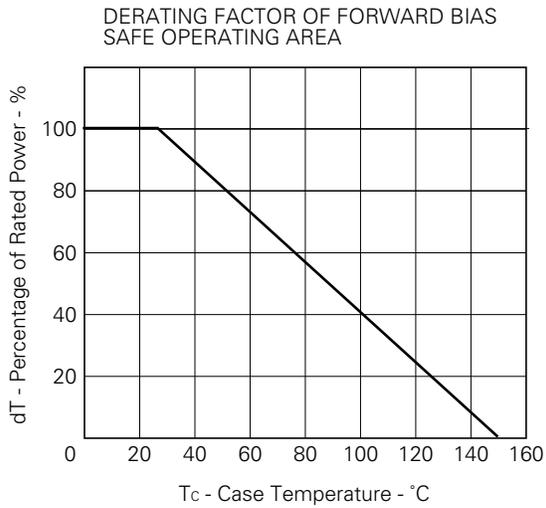


Test Circuit 3 Gate Charge

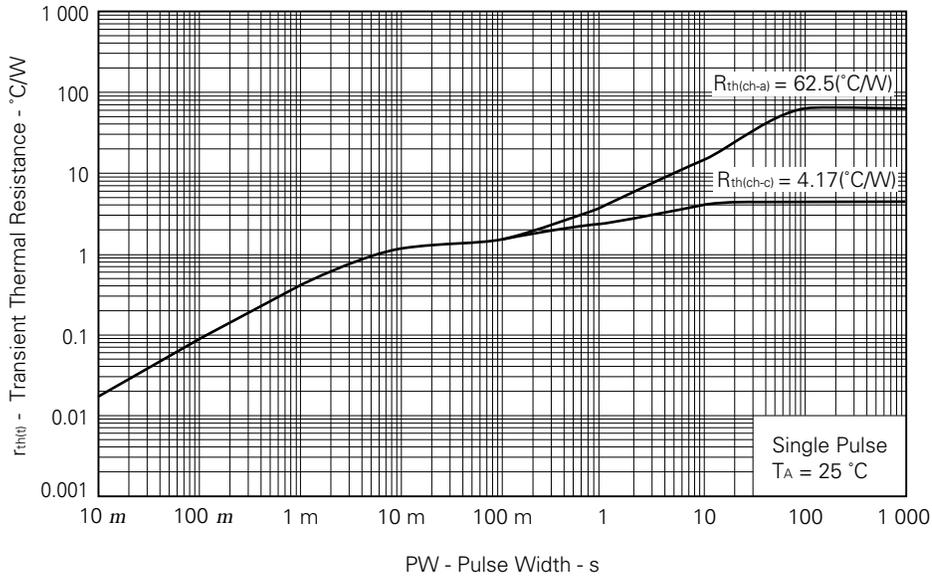


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

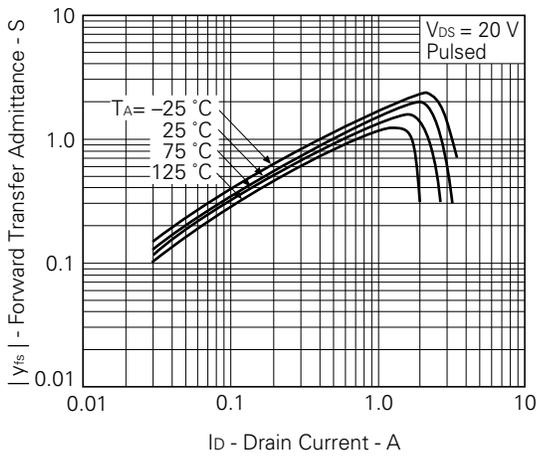
TYPICAL CHARACTERISTICS (T_A = 25 °C)



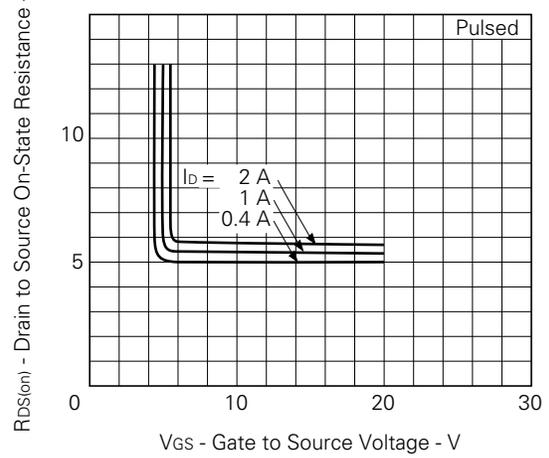
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



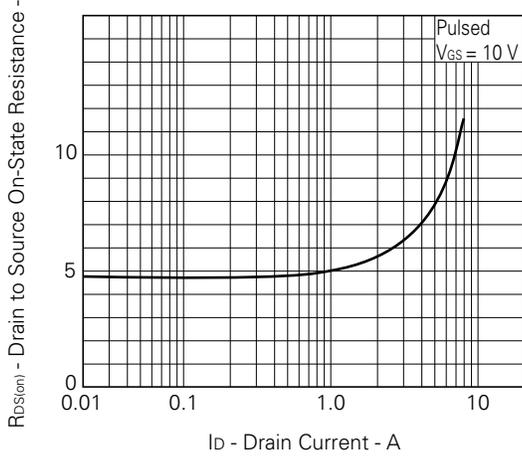
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



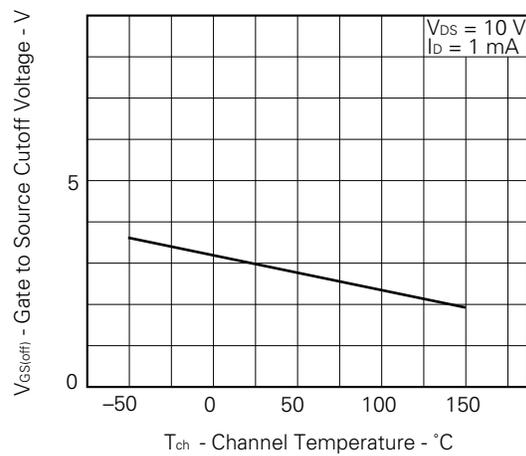
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



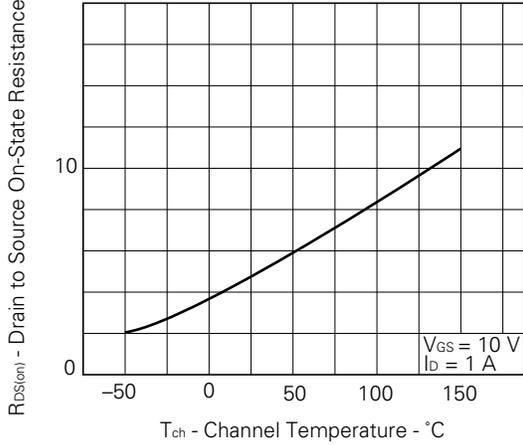
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



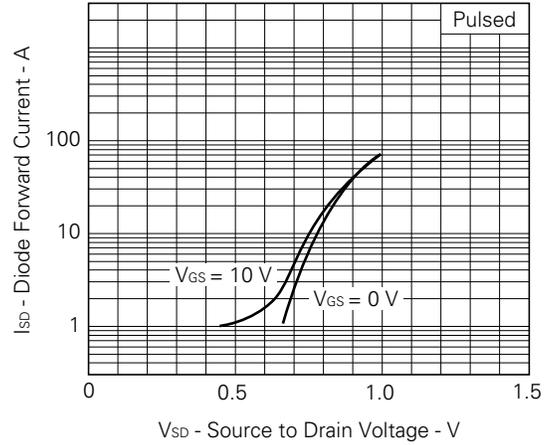
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



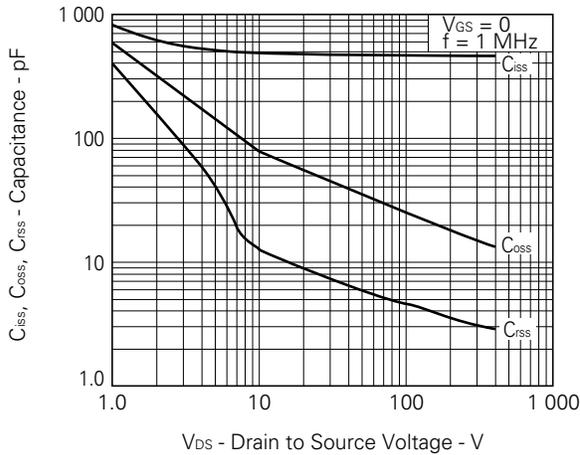
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



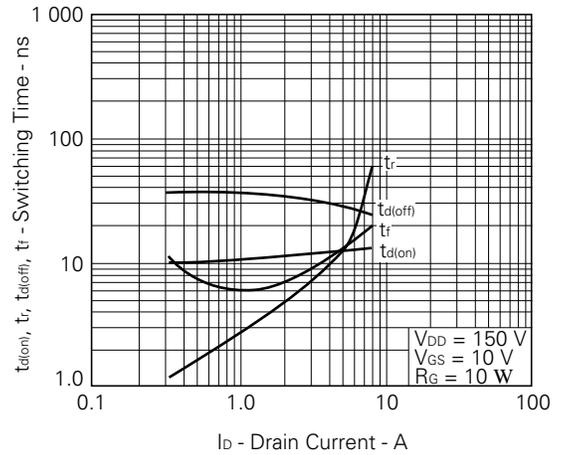
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



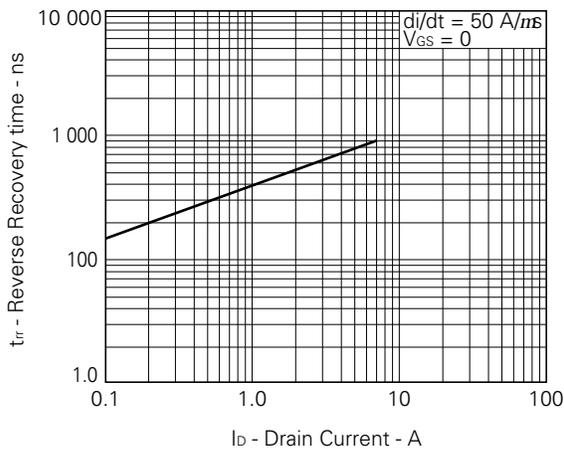
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



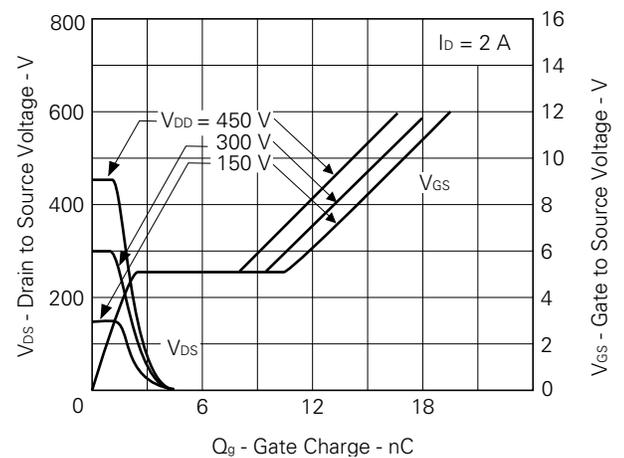
SWITCHING CHARACTERISTICS



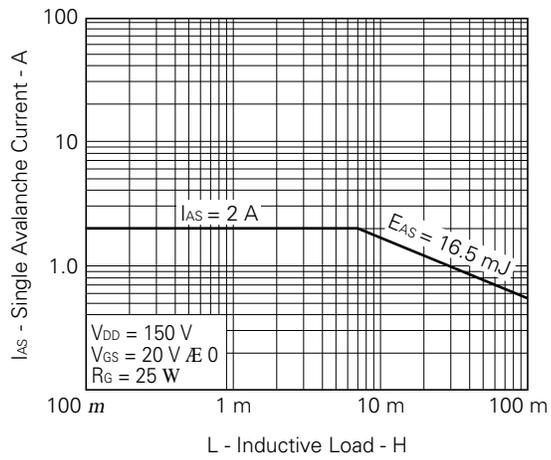
REVERSE RECOVERY TIME vs. DRAIN CURRENT



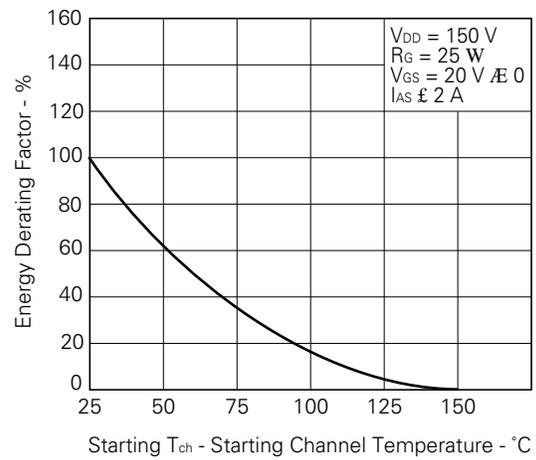
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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Anti-radioactive design is not implemented in this product.