DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR

2SK2488

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK2488 is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-Resistance
  $R_{DS(on)} = 1.2\ \Omega$ ($V_{GS} = 10$ V, $I_D = 5.0$ A)
- Low C_{iss} $C_{iss} = 2\,900$ pF TYP.
- High Avalanche Capability Ratings

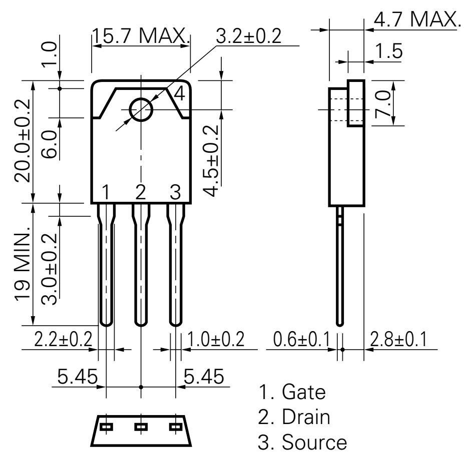
ABSOLUTE MAXIMUM RATINGS ($T_A = 25\ ^\circ C$)

Drain to Source Voltage	V_{DSS}	900	V
Gate to Source Voltage	V_{GSS}	±30	V
Drain Current (DC)	$I_{D(DC)}$	±10	A
Drain Current (pulse)*	$I_{D(pulse)}$	±20	A
Total Power Dissipation ($T_c = 25\ ^\circ C$)	P_{T1}	150	W
Total Power Dissipation ($T_A = 25\ ^\circ C$)	P_{T2}	3.0	W
Channel Temperature	T_{ch}	150	˚C
Storage Temperature	T_{stg}	–55 to +150	˚C
Single Avalanche Current**	I_{AS}	10	A
Single Avalanche Energy**	E_{AS}	294	mJ

* PW ≤ 10 μs, Duty Cycle ≤ 1 %

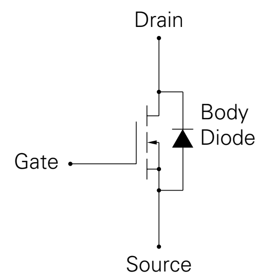
** Starting $T_{ch} = 25\ ^\circ C$, $R_G = 25\ \Omega$, $V_{GS} = 20\ V \rightarrow 0$

PACKAGE DIMENSIONS
(in millimeter)



1. Gate
2. Drain
3. Source
4. Fin (Drain)

MP-88

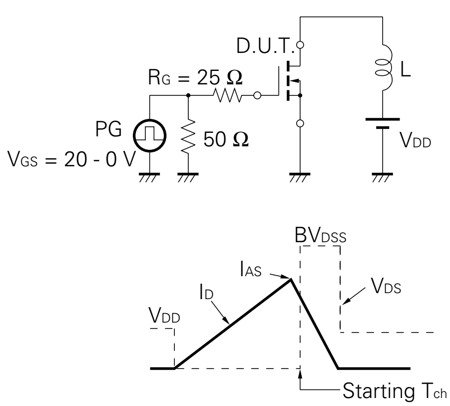


Document No. D10284EJ1V0DS00 (1st edition)
Date Published August 1995 P
Printed in Japan

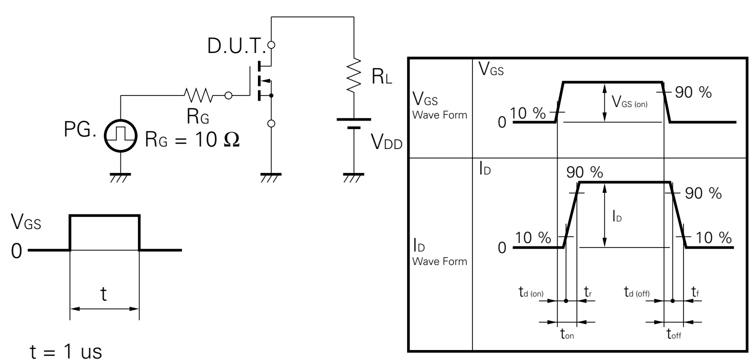
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	$R_{DS (on)}$		1.0	1.2	Ω	V_{GS} = 10 V, I_D = 5.0 A
Gate to Source Cutoff Voltage	$V_{GS (off)}$	2.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\mid y_{fs} \mid$	3.5			S	V_{DS} = 20 V, I_D = 5.0 A
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = V_{DSS}, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±30 V, V_{DS} = 0
Input Capacitance	C_{iss}		2 900		pF	V_{DS} = 10 V
Output Capacitance	C_{oss}		400		pF	V_{GS} = 0
Reverse Transfer Capacitance	C_{rss}		70		pF	f = 1 MHz
Turn-On Delay Time	$t_{d (on)}$		35		ns	I_D = 5.0 A
Rise Time	t_r		30		ns	V_{GS} = 10 V
Turn-Off Delay Time	$t_{d (off)}$		160		ns	V_{DD} = 150 V
Fall Time	t_f		32		ns	R_G = 10 Ω
Total Gate Charge	Q_G		90		nC	I_D = 10 A
Gate to Source Charge	Q_{GS}		16		nC	V_{DD} = 450 V
Gate to Drain Charge	Q_{GD}		40		nC	V_{GS} = 10 V
Body Diode Forward Voltage	$V_{F (S-D)}$		1.0		V	I_F = 10 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		990		ns	I_F = 10 A, V_{GS} = 0
Reverse Recovery Charge	Q_{rr}		7.0		μC	di/dt = 50 A/μs

Test Circuit 1 Avalanche Capability

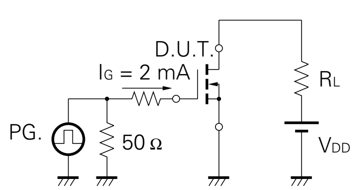


Test Circuit 2 Switching Time



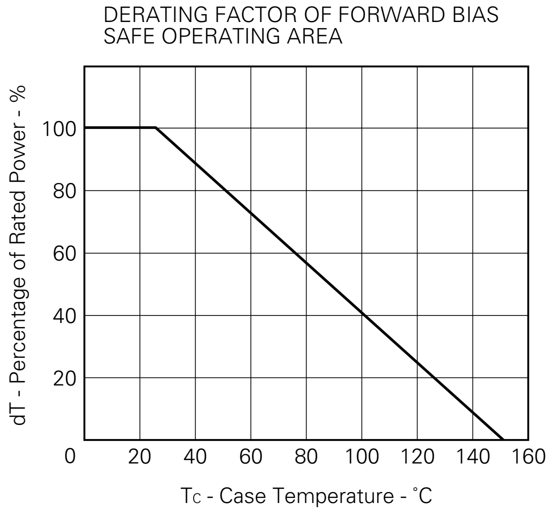
t = 1 us
Duty Cycle ≤ 1 %

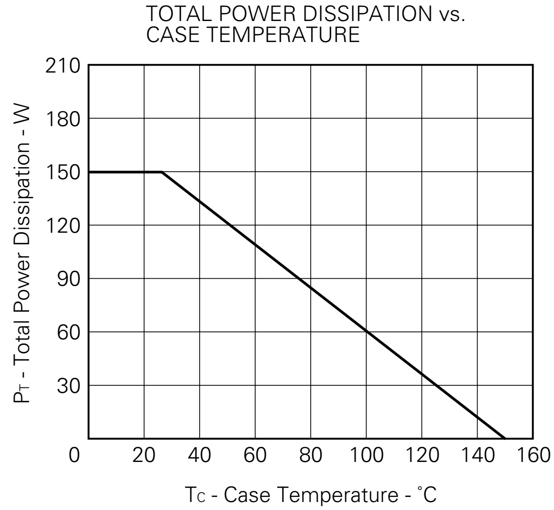
Test Circuit 3 Gate Charge

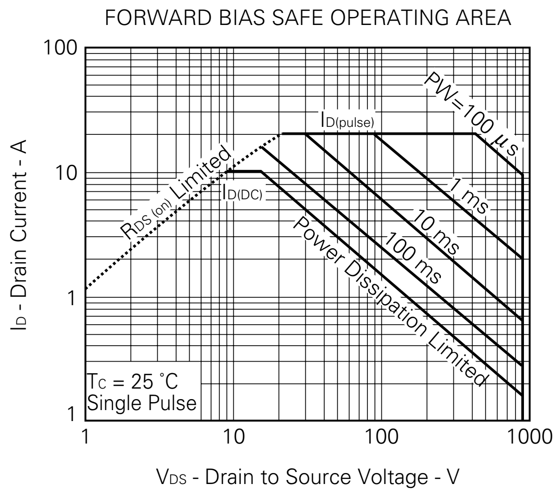


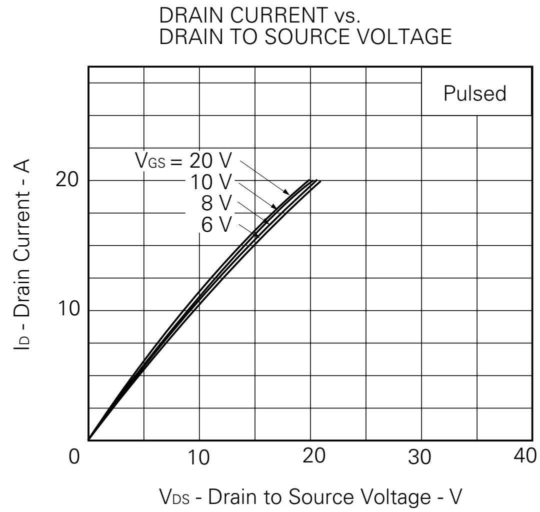
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

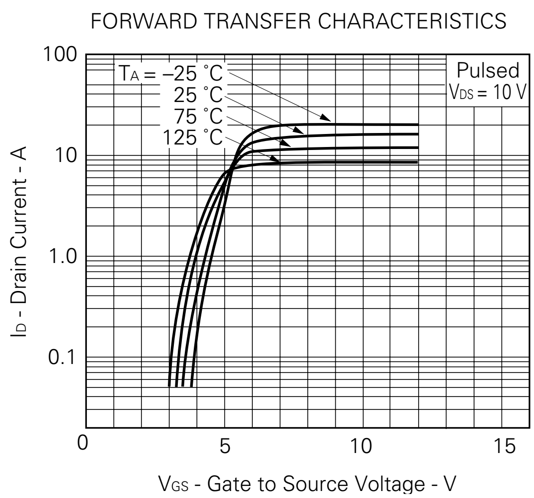
TYPICAL CHARACTERISTICS (T_A = 25 °C)



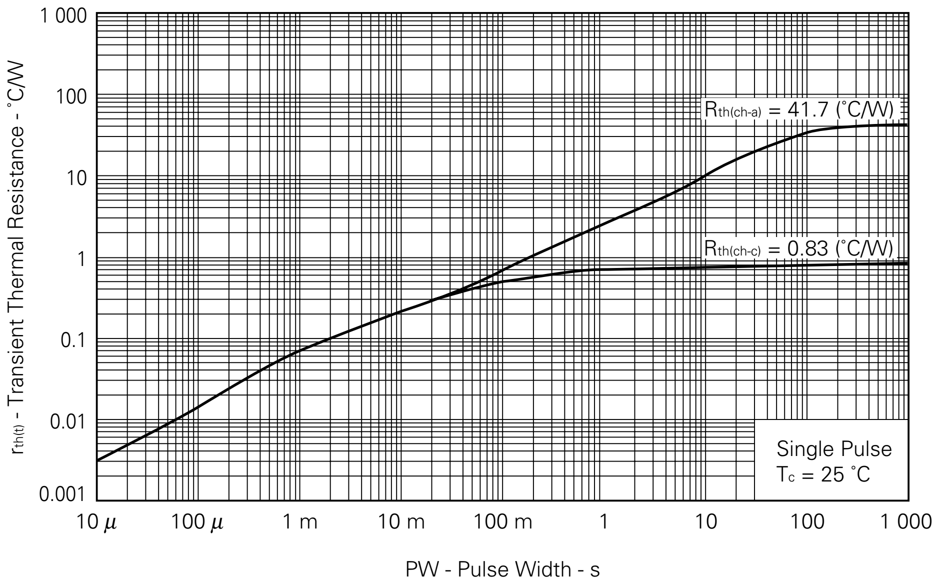




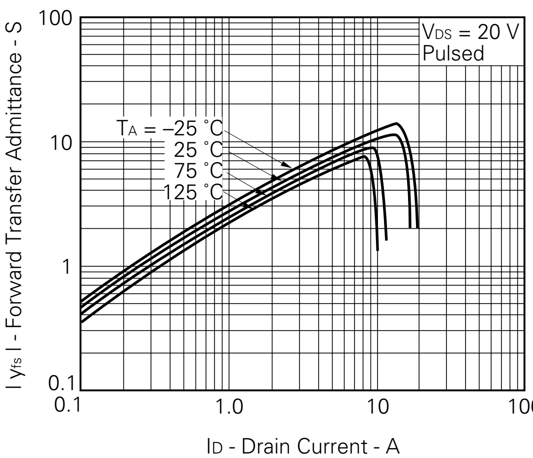




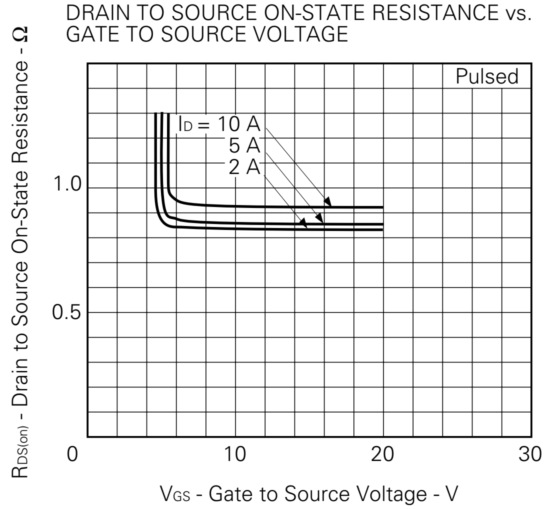
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



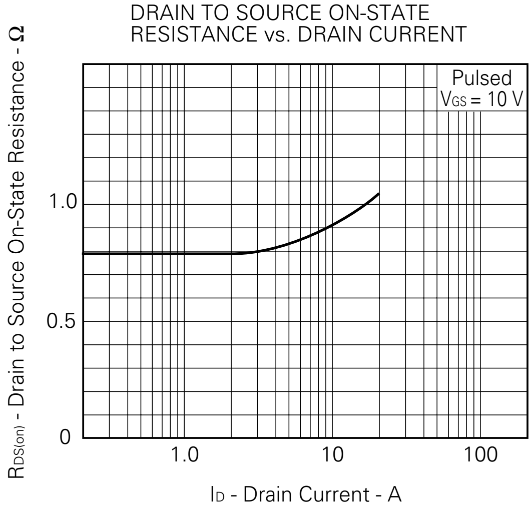
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



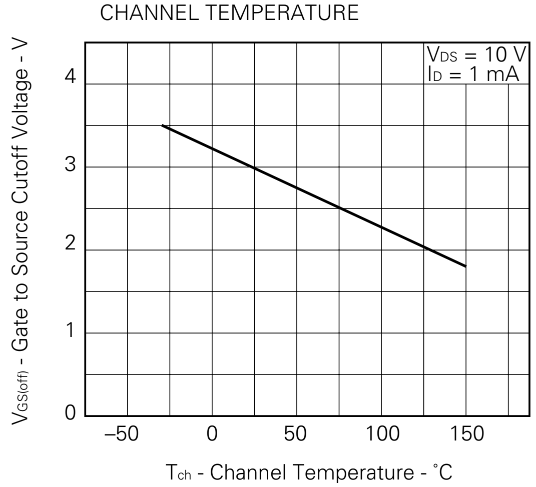
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



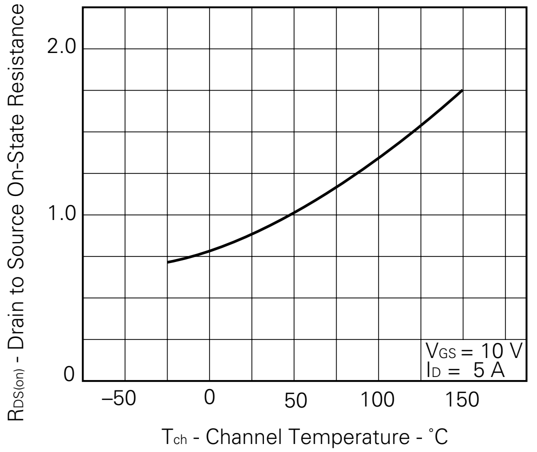
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



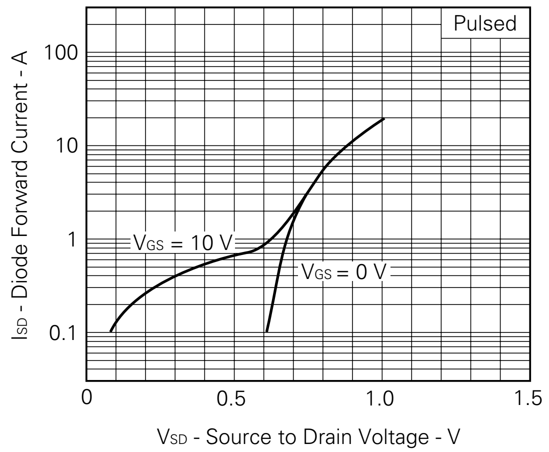
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



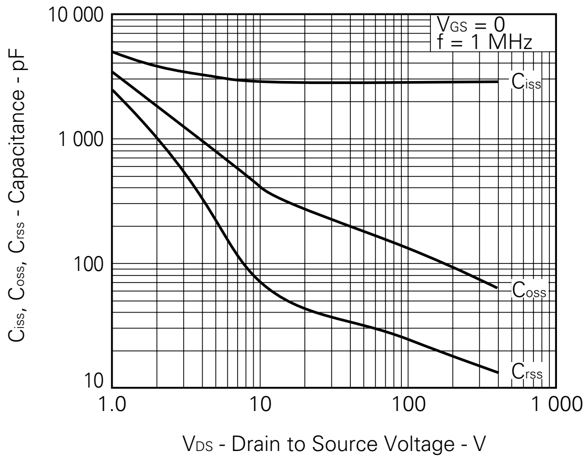
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



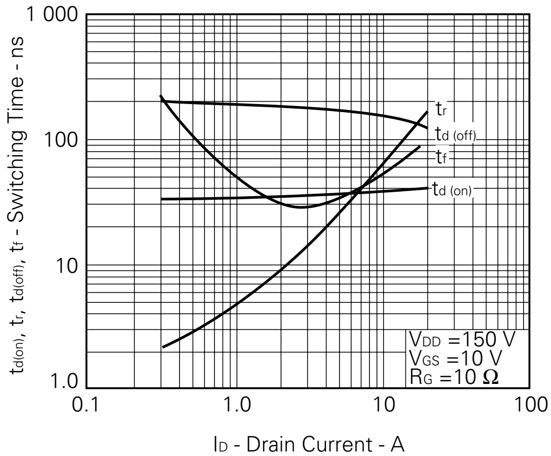
SOURCE TO DRAIN DIODE
FORWARD VOLTAGE



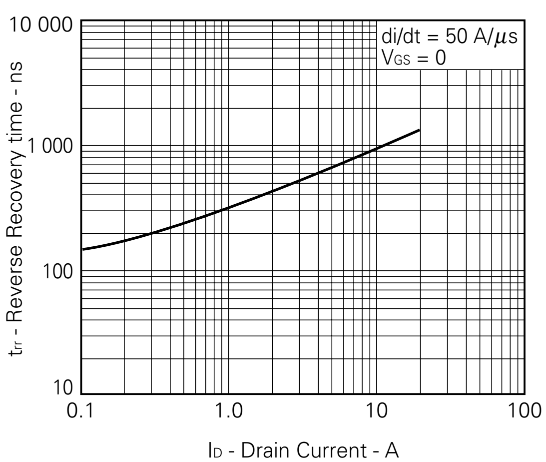
CAPACITANCE vs. DRAIN TO
SOURCE VOLTAGE



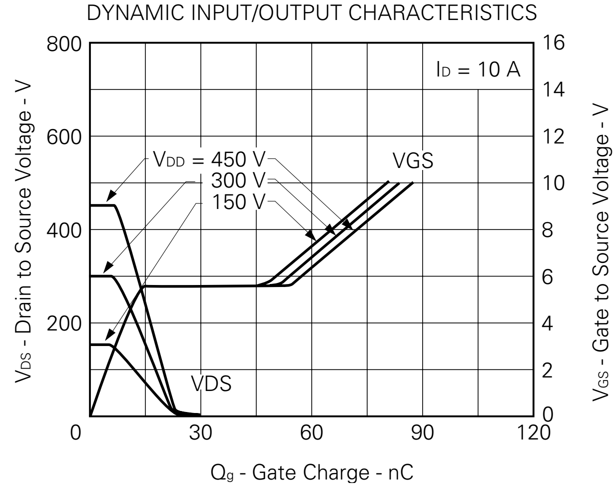
SWITCHING CHARACTERISTICS



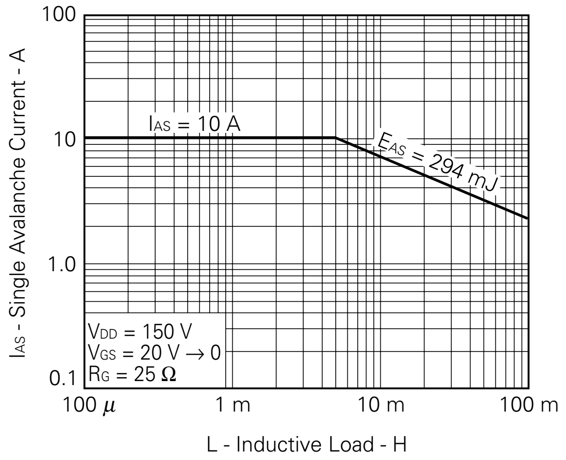
REVERSE RECOVERY TIME vs.
DRAIN CURRENT



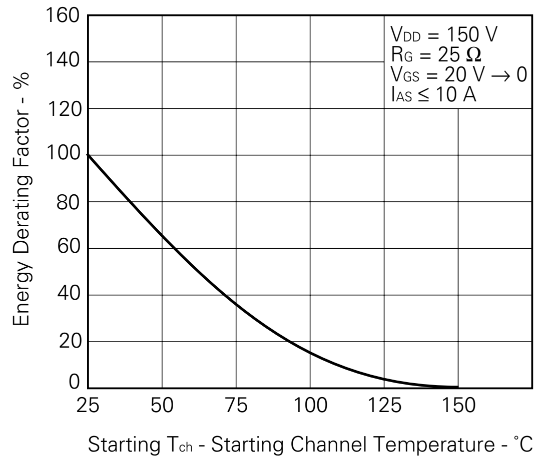
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

[MEMO]