NEC

MOS FIELD EFFECT TRANSISTOR
2SK3111

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK3111 is N channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter, actuator driver.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3111	TO-220AB
2SK3111-S	TO-262
2SK3111-ZJ	TO-263

FEATURES

- Gate voltage rating ±30 V
- Low on-state resistance
  $R_{DS(on)}$ = 180 mΩ MAX. (V_{GS} = 10 V, I_D = 10 A)
- Low input capacitance
  C_{iss} = 1000 pF TYP. (V_{DS} = 10 V, V_{GS} = 0 V)
- Avalanche capability rated
- Built-in gate protection diode
- Surface mount device available

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to source voltage (V_{GS} = 0 V)	V_{DSS}	200	V
Gate to source voltage (V_{DS} = 0 V)	V_{GSS}	±30	V
Drain current (DC) (T_C = 25 °C)	$I_{D(DC)}$	±20	A
Drain current (pulse) **Note1**	$I_{D(pulse)}$	±60	A
Total power dissipation (T_A = 25 °C)	P_{T1}	1.5	W
Total power dissipation (T_C = 25 °C)	P_{T2}	65	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	–55 to +150	°C
Single avalanche current **Note2**	I_{AS}	20	A
Single avalanche energy **Note2**	E_{AS}	100	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. Starting T_{ch} = 25 °C, V_{DD} = 100 V, R_G = 25 Ω, V_{GS} = 20 V→0 V

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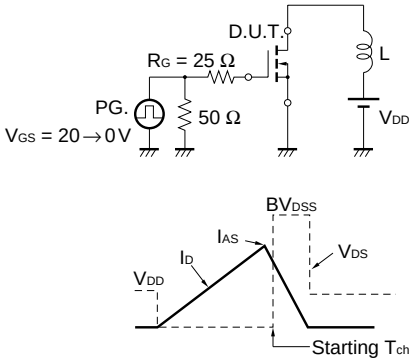
The mark ★ shows major revised points.

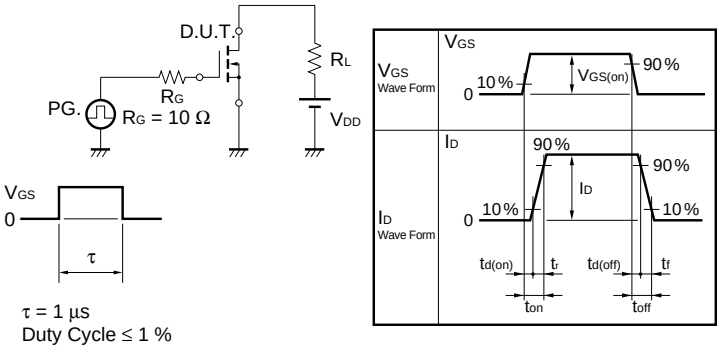
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain Leakage Current	I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V			100	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	2.5		4.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 10 A	3.0			S
Drain to Source On-state Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A		120	180	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		1000		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		300		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		150		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 100 V		25		ns
Rise Time	t_r	I_D = 10 A		90		ns
Turn-off Delay Time	$t_{d(off)}$	$V_{GS(on)}$ = 10 V		80		ns
Fall Time	t_f	R_G = 10 Ω		40		ns
Total Gate Charge	Q_G	V_{DD} = 160 V		40		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		7		nC
Gate to Drain Charge	Q_{GD}	I_D = 20 A		25		nC
Diode Forward Voltage	$V_{F(S-D)}$	I_F = 20 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 20 A, V_{GS} = 0 V		300		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/μs		1.7		μC

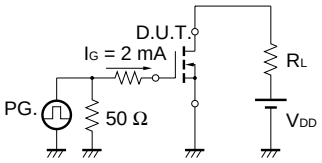
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

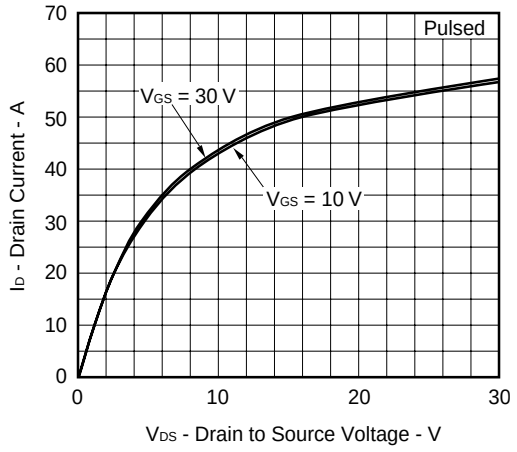


TEST CIRCUIT 3 GATE CHARGE

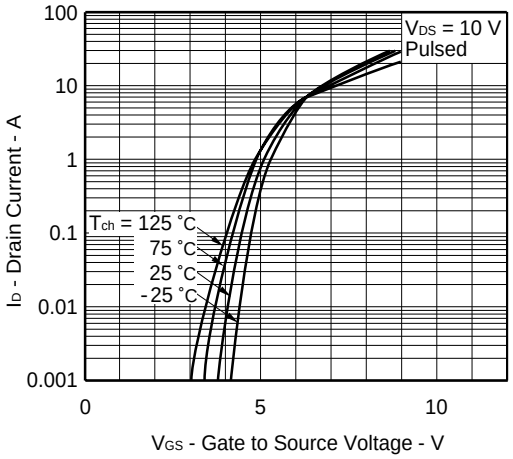


TYPICAL CHARACTERISTICS (T_A = 25°C)

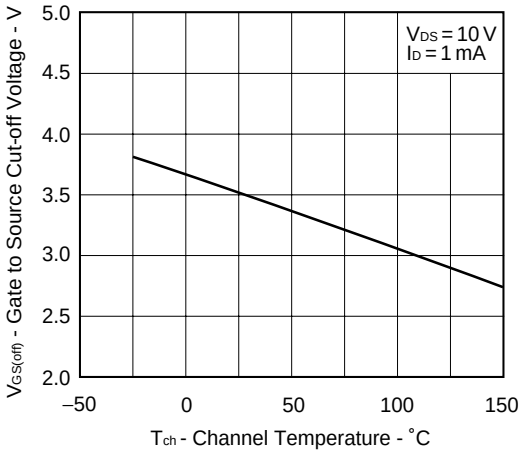
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



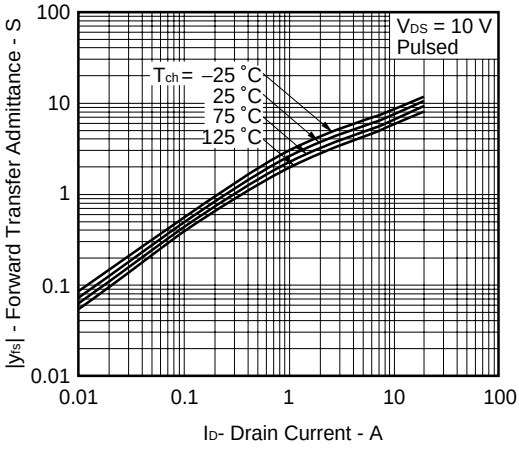
FORWARD TRANSFER CHARACTERISTICS



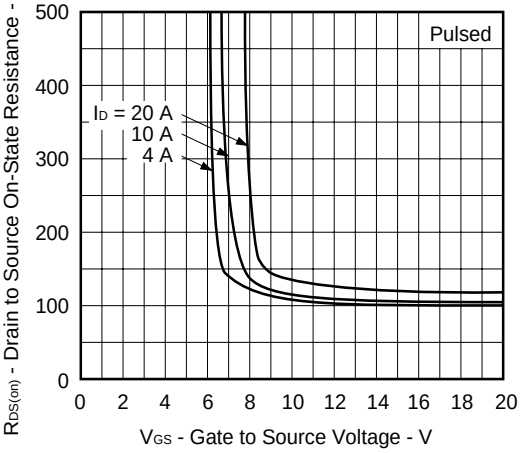
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



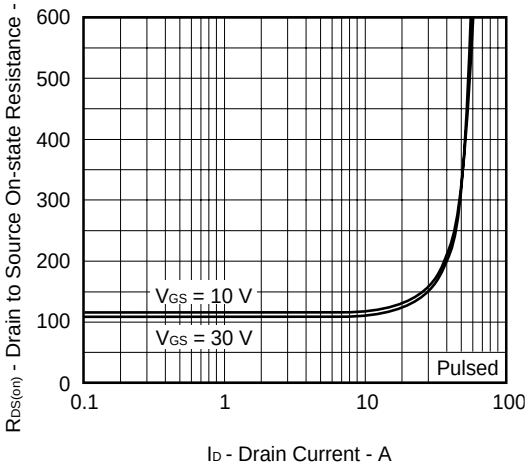
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



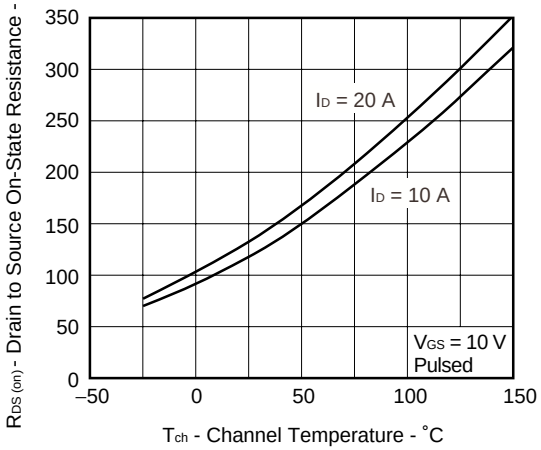
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



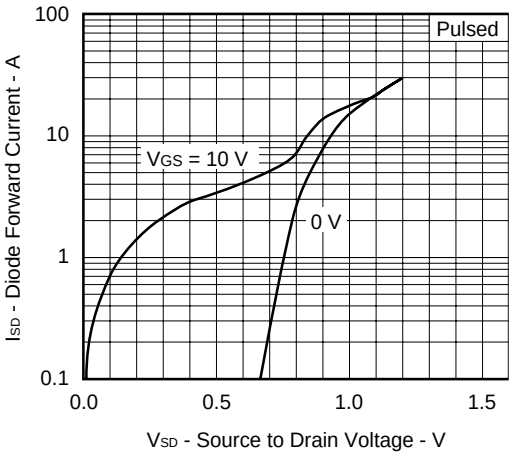
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



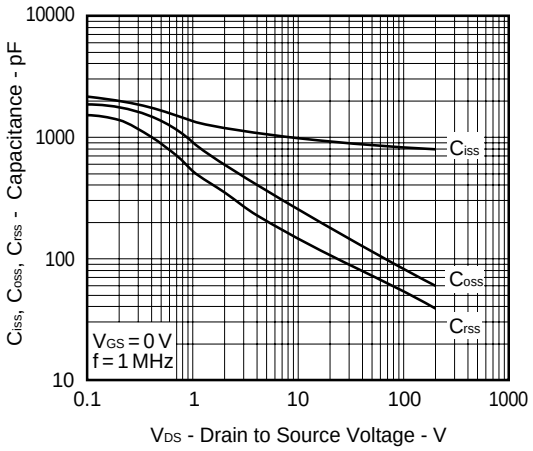
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



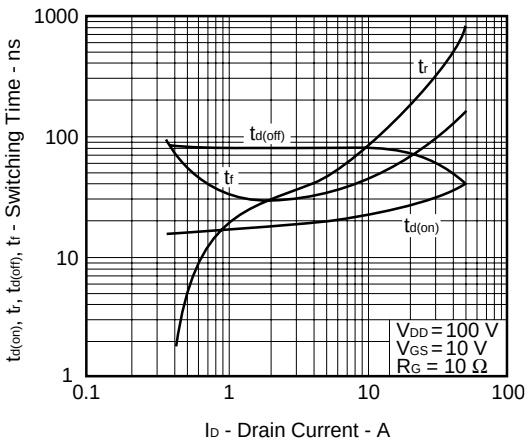
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



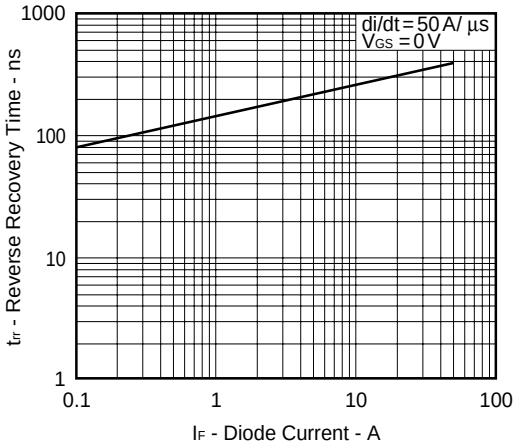
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



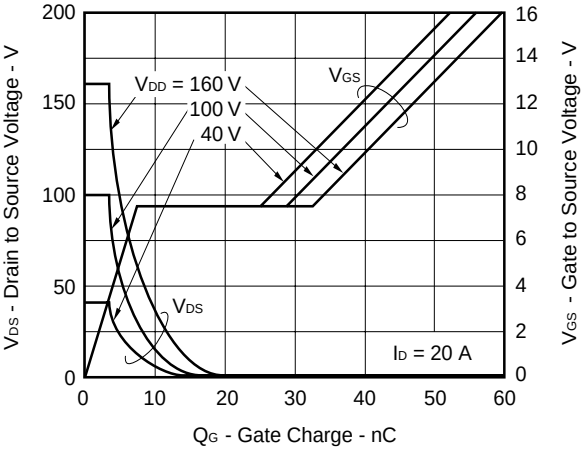
SWITCHING CHARACTERISTICS



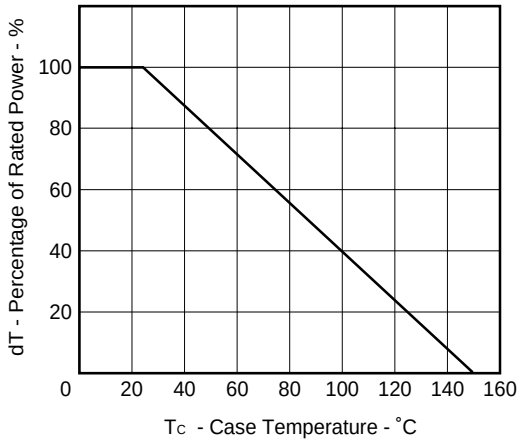
REVERSE RECOVERY TIME vs. DIODE CURRENT



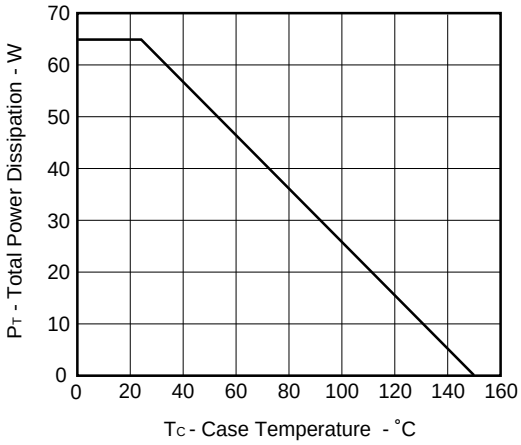
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



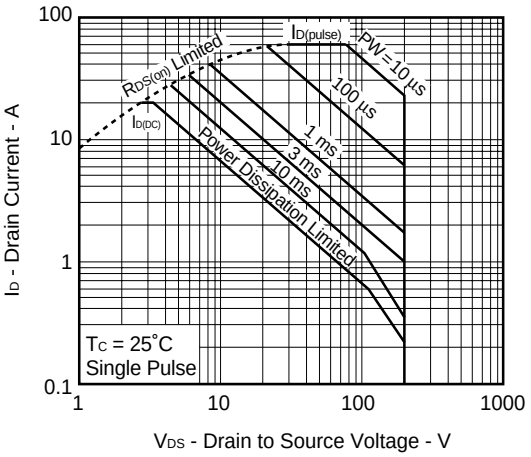
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



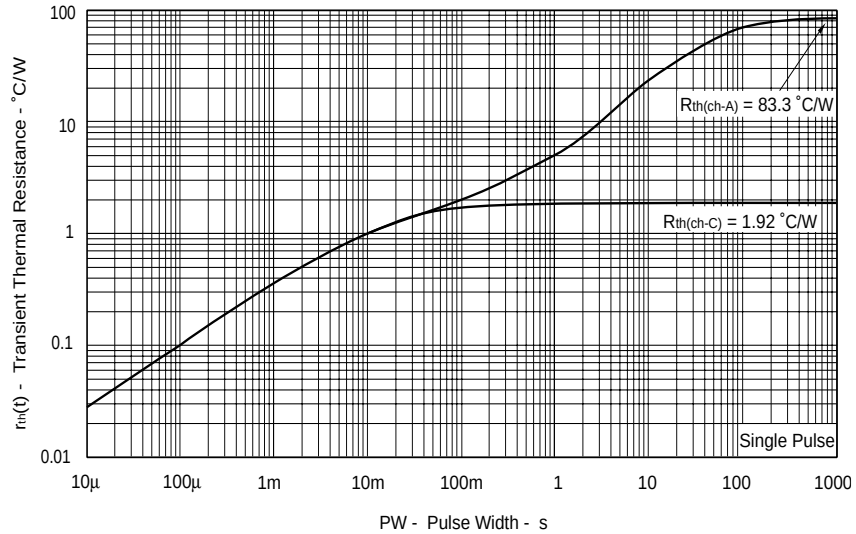
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



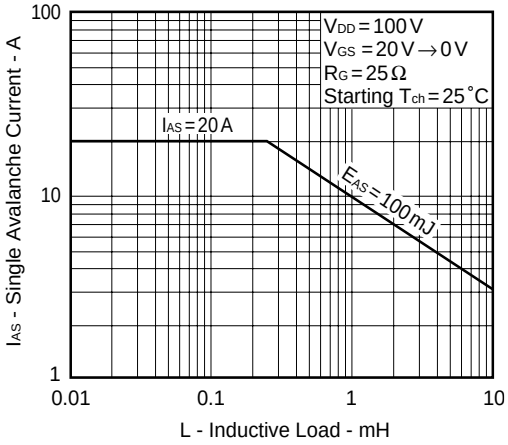
★ FORWARD BIAS SAFE OPERATING AREA



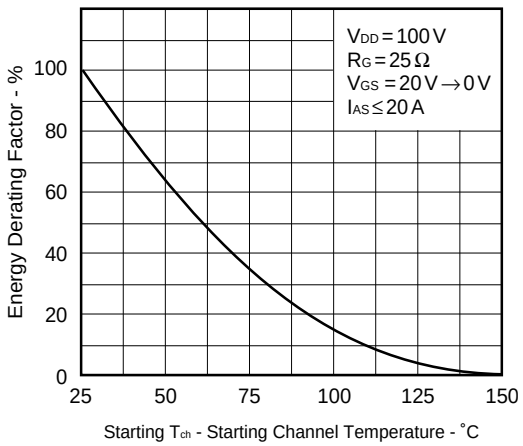
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



★ SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

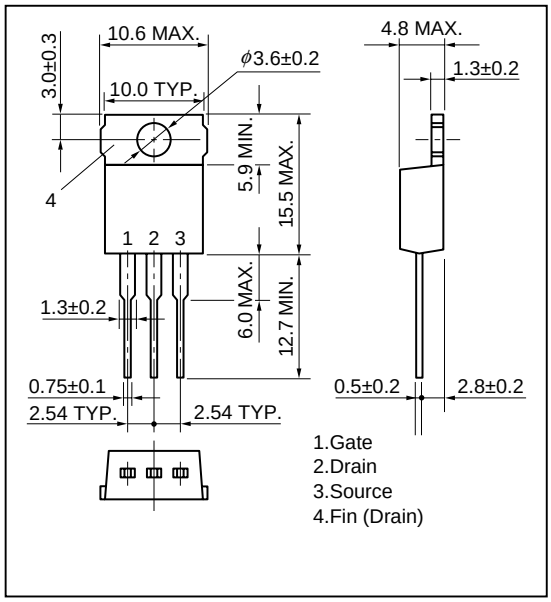


SINGLE AVALANCHE ENERGY DERATING FACTOR

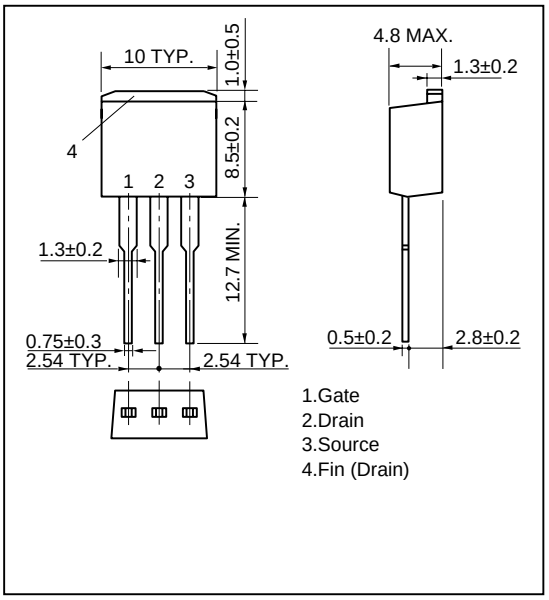


★ PACKAGE DRAWINGS (Unit : mm)

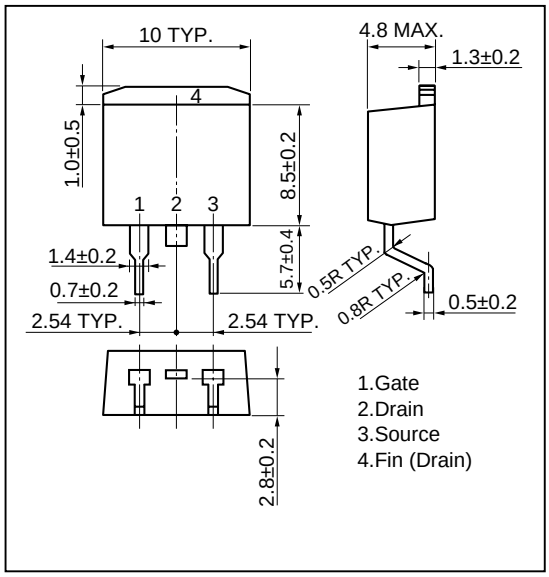
1)TO-220AB (MP-25)



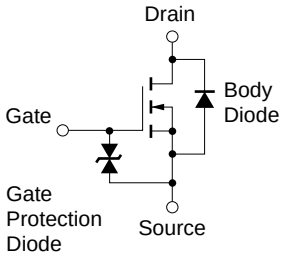
2)TO-262 (MP-25 Fin Cut)



3)TO-263 (MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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