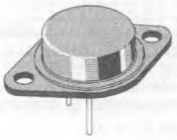
SGS-THOMSON MICROELECTRONICS

BUW34/BUW35 BUW36

HIGH VOLTAGE POWER SWITCH

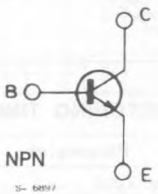
DESCRIPTION

The BUW34, BUW35 and BUW36 are silicon multiepitaxial mesa NPN transistors in Jedec TO-3 metal case. They are intended for high voltage, fast switching applications.



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		BUW34	BUW35	BUW36	
V_{CES}	Collector-emitter Voltage (V_{BE} = 0)	500	800	900	V
V_{CEO}	Collector-emitter Voltage (I_B = 0)	400	400	450	V
V_{EBO}	Emitter-base Voltage (I_C = 0)	7			V
I_C	Collector Current	10			A
I_{CM}	Collector Peak Current	15			A
I_B	Base Current	5			A
P_{tot}	Total Power Dissipation at $T_{case} \leq 25$ °C	125			W
T_{stg}	Storage Temperature	– 65 to 200			°C
T_j	Junction Temperature	200			°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	max	1.4	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cutoff Current (V_{BE} = 0)	for **BUW34** V_{CE} = 500 V			500	µA
		for **BUW35** V_{CE} = 800 V			500	µA
		for **BUW36** V_{CE} = 900 V			500	µA
		T_{case} = 125 °C				
		for **BUW34** V_{CE} = 500 V			3	mA
		for **BUW35** V_{CE} = 800 V			3	mA
		for **BUW36** V_{CE} = 900 V			3	mA
I_{EBO}	Emitter Cutoff Current (I_C = 0)	V_{EB} = 7 V			1	mA
$V_{CEO(sus)}$*	Collector-emitter Sustaining Voltage (I_B = 0)	I_C = 100 mA				
		for **BUW34**	400			V
		for **BUW35**	400			V
		for **BUW36**	450			V
$V_{CE(sat)}$*	Collector-emitter Saturation Voltage	All Types I_C = 5 A, I_B = 1 A			1.5	V
		for **BUW35** I_C = 8 A, I_B = 2.5 A			1.5	V
		for **BUW36** I_C = 8 A, I_B = 2.5 A			3	V
$V_{BE(sat)}$*	Base-emitter Saturation Voltage	All Types I_C = 5 A, I_B = 1 A			1.5	V
		for **BUW35** I_C = 8 A, I_B = 2.5 A			1.8	V
		for **BUW36** I_C = 8 A, I_B = 2.5 A			1.8	V

RESISTIVE SWITCHING TIMES (see fig. 1)

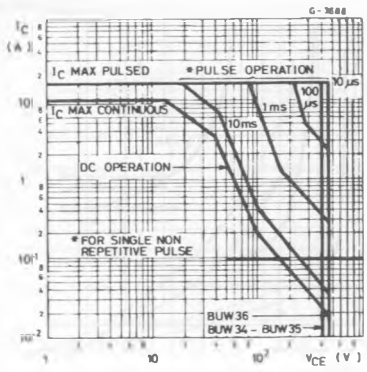
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{on}	Turn-on Time	I_C = 5 A, I_{B1} = 1 A, V_{CC} = 250 V			0.70	µs
ts	Storage Time	I_C = 5 A, I_{B1} = 1 A, I_{B2} = − 1 A, V_{CC} = 250 V			3	µs
t_f	Fall Time				0.8	µs

INDUCTIVE SWITCHING TIMES (see fig. 2)

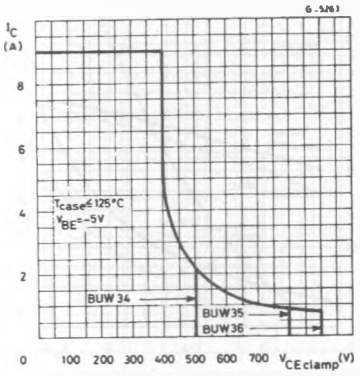
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_f	Fall Time	I_C = 5 A, I_{B1} = 1 A, V_{BE} = − 5 V, V_{CC} = 300 V, T_{case} = 100 °C			0.3	µs
		I_C = 5 A, I_{B1} = 1 A, V_{BE} = − 5 V, V_{CC} = 300 V			0.6	µs

* Pulsed : pulse duration ≤ 300 µs, duty cycle ≤ 1.5 %.

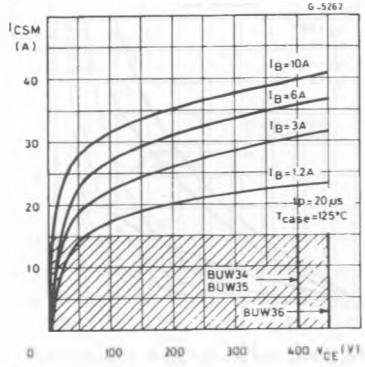
Safe Operating Areas.



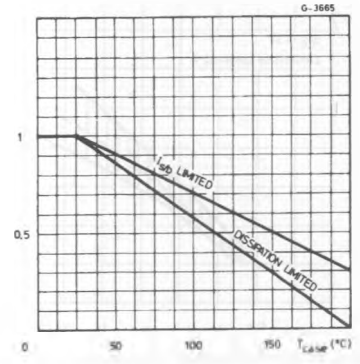
Clamped Reverse Bias Safe Operating Areas.



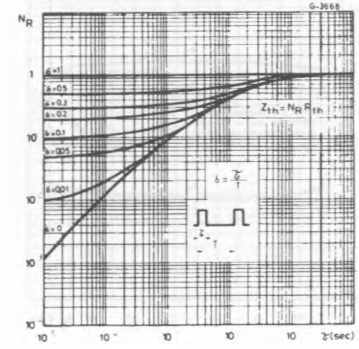
Forward Biased Accidental Overload Area (see fig. 3).



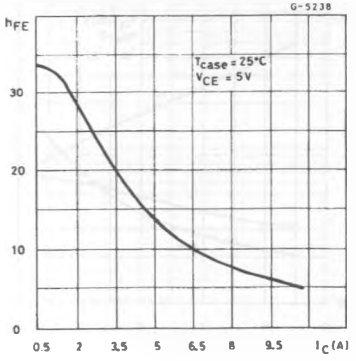
Derating Curves.



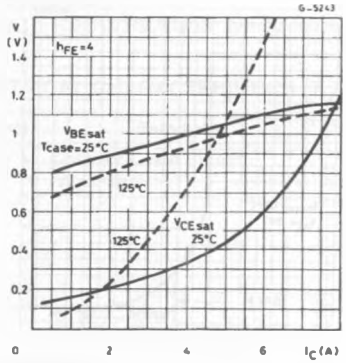
Transient Thermal Response.



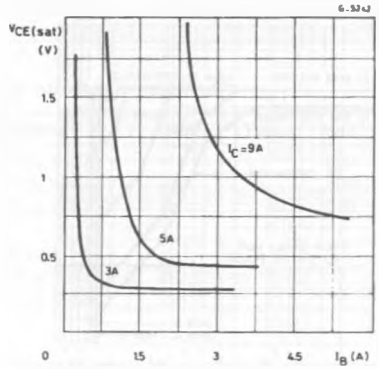
DC Current Gain.



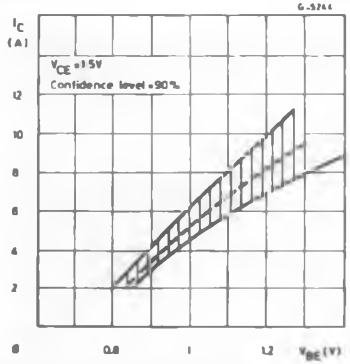
Saturation Voltages.



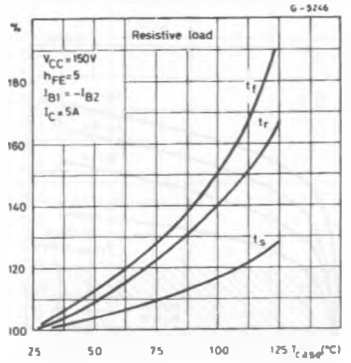
Collector-emitter Saturation Voltage.



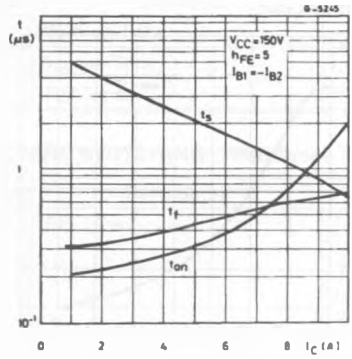
Collector Current Spread vs. Base Emitter Voltage.



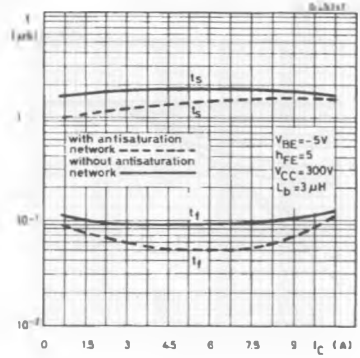
Switching Time Percentage Variation vs. case Temperature.



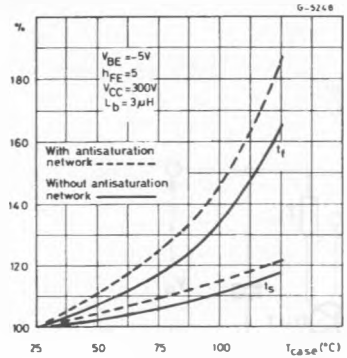
Switching Times Resistive Load (see fig. 1).



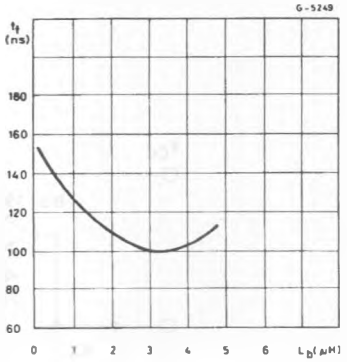
Switching Time Inductive Load (see fig. 2).



Switching Time Inductive Load vs. Case Temperature.



Fall Times vs. L_B (see fig. 2).



Dynamic Collector-emitter Saturation Voltage (see fig. 4).

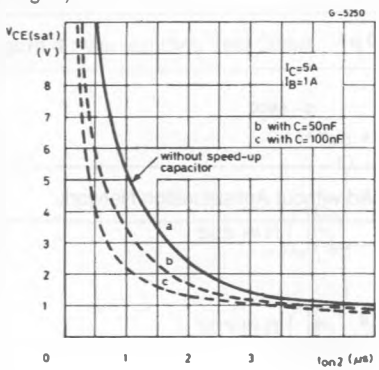


Figure 1 : Switching Times Test Circuit on resistive Load.

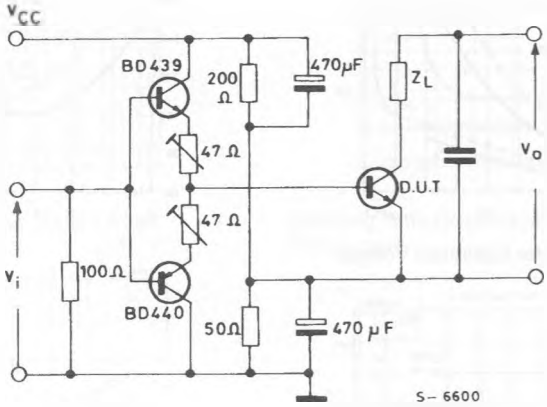
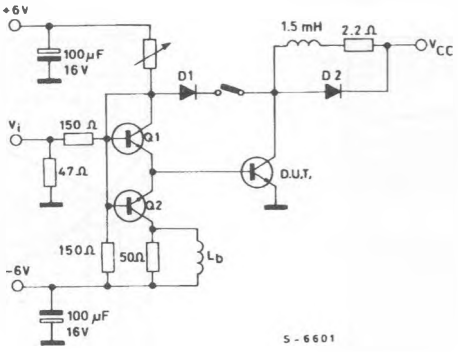


Figure 2 : Switching Times Test Circuit on Inductive Load with Ad without Antisaturation Network.



D1, D2 - Fast recovery diodes
Q1, Q2 - Transistors SGS: 2N5191, 2N5195.

Figure 3 : Forward Biased Accidental Over Load Area Test Circuit.

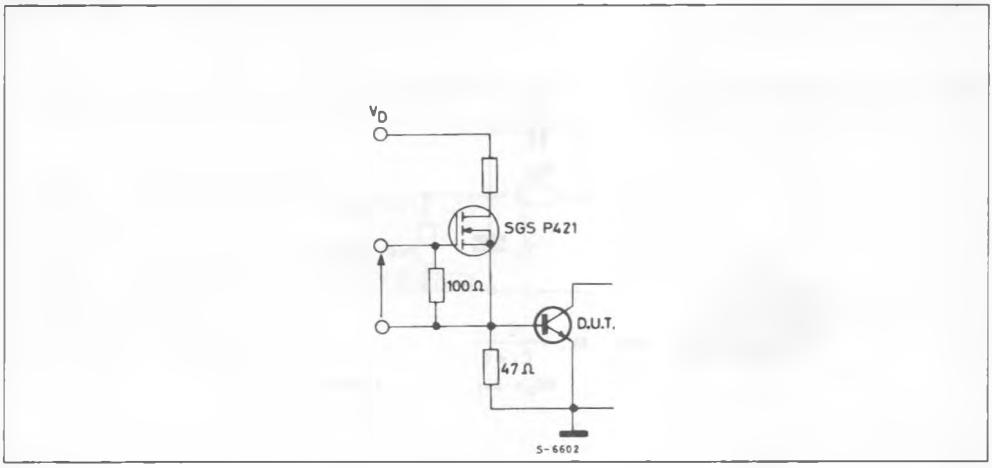


Figure 4 : $V_{CE\ (sat)}$ Dyn. Test Circuit.

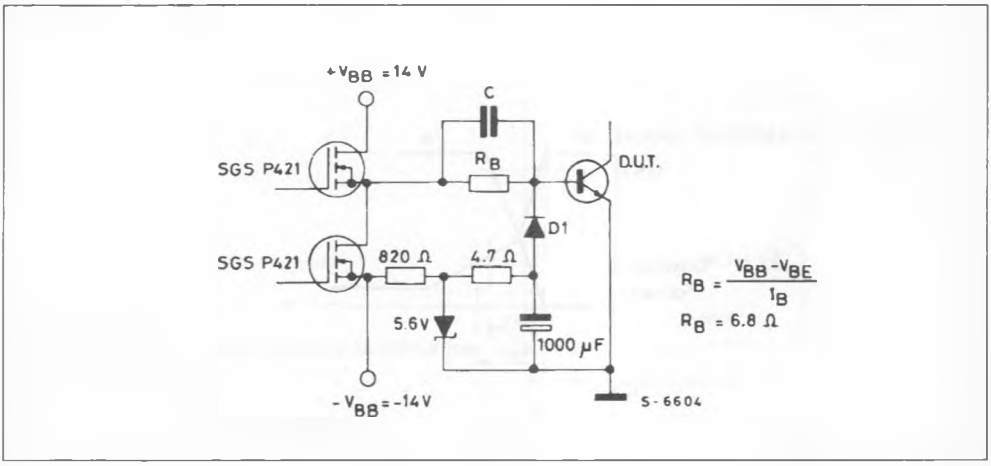


Figure 5 : Equivalent Input Schematic at Turn-on.

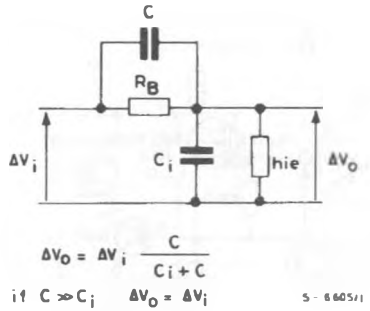
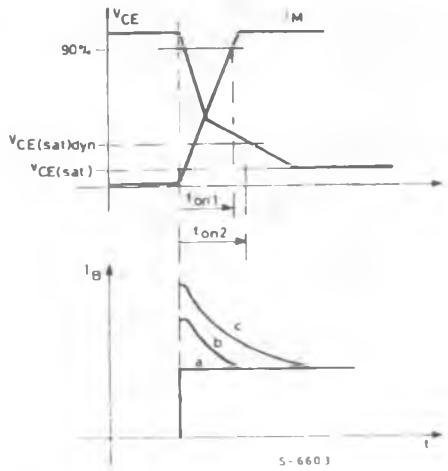


Figure 6 : Remarks to $V_{CE\ (sat)}$ Dyn. Test Circuit (fig. 4).



The speed-up capacitor decreases the $V_{CE\ (sat)}$ dyn. as shown in diagram (figure 6). The 50 nF capacitor modifies the shape of base current with a overshoot.