CMLDM7002A
CMLDM7002AJ*

SURFACE MOUNT PICOmini™
DUAL N-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET

PICOmini™

SOT-563 CASE

Central™
Semiconductor Corp.

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CMLDM7002A and CMLDM7002AJ are special dual versions of the 2N7002 Enhancement-mode N-Channel Field Effect Transistor, manufactured by the N-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. The CMLDM7002A utilizes the USA pinout configuration, while the CMLDM7002AJ utilizes the Japanese pinout configuration. These special Dual Transistor devices offers low $r_{DS(ON)}$ and low $V_{DS\ (ON)}$.

MARKING CODE: CMLDM7002A: L02
CMLDM7002AJ*: 02J * Preliminary

MAXIMUM RATINGS (T_A=25°C)

	SYMBOL		UNITS
Drain-Source Voltage	V_{DS}	60	V
Drain-Gate Voltage	V_{DG}	60	V
Gate-Source Voltage	V_{GS}	40	V
Continuous Drain Current	I_D	280	mA
Continuous Source Current (Body Diode)	I_S	280	mA
Maximum Pulsed Drain Current	I_{DM}	1.5	A
Maximum Pulsed Source Current	I_{SM}	1.5	A
Power Dissipation	P_D	350	mW
Operating and Storage Junction Temperature	T_J,T_{stg}	-65 to +150	°C
Thermal Resistance	Θ_{JA}	357	°C/W

ELECTRICAL CHARACTERISTICS PER TRANSISTOR (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{GSSF}	V_{GS}=20V, V_{DS}=0V		100	nA
I_{GSSR}	V_{GS}=20V, V_{DS}=0V		100	nA
I_{DSS}	V_{DS}=60V, V_{GS}=0V		1.0	μA
I_{DSS}	V_{DS}=60V, V_{GS}=0V, T_j=125°C		500	μA
$I_{D(ON)}$	V_{GS}=10V, $V_{DS} \geq 2V_{DS(ON)}$	500		mA
BV_{DSS}	V_{GS}=0V, I_D=10μA	60		V
$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.0	2.5	V
$V_{DS(ON)}$	V_{GS}=10V, I_D=500mA		1.0	V
$V_{DS(ON)}$	V_{GS}=5.0V, I_D=50mA		0.15	V
$r_{DS(ON)}$	V_{GS}=10V, I_D=500mA		2.0	Ω
$r_{DS(ON)}$	V_{GS}=10V, I_D=500mA, T_j=125°C		3.5	Ω
$r_{DS(ON)}$	V_{GS}=5.0V, I_D=50mA		3.0	Ω
$r_{DS(ON)}$	V_{GS}=5.0V, I_D=50mA, T_j=125°C		5.0	Ω
g_{FS}	$V_{DS} \geq 2V_{DS(ON)}$, I_D=200mA	80		mmhos
C_{rss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz		5.0	pF
C_{iss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz		50	pF
C_{oss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz		25	pF
t_{on}	V_{DD}=30V, V_{GS}=10V, I_D=200mA,		20	ns
t_{off}	R_G=25Ω, R_L=150Ω		20	ns
V_{SD}	V_{GS}=0V, I_S=400mA		1.2	V

R1 (20-February 2003)

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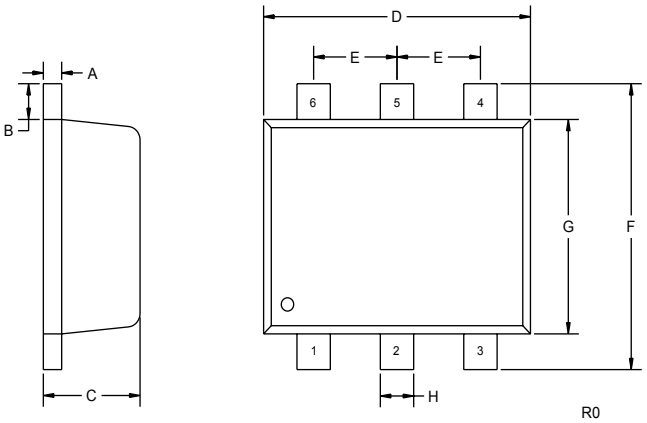
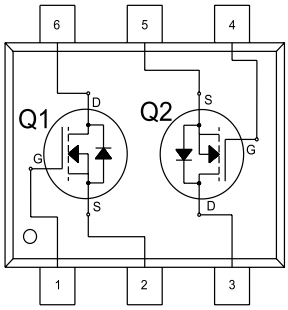
SOT-563 CASE - MECHANICAL OUTLINE



DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.004	0.007	0.10	0.18
B	0.008		0.20	
C	0.022	0.024	0.56	0.60
D	0.059	0.067	1.50	1.70
E	0.020		0.50	
F	0.061	0.067	1.55	1.70
G	0.047		1.20	
H	0.006	0.012	0.15	0.30

SOT-563 (REV: R0)

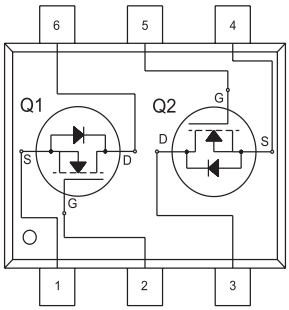
CMLDM7002A
(USA Pinout)



LEAD CODE:
1) GATE Q1
2) SOURCE Q1
3) DRAIN Q2
4) GATE Q2
5) SOURCE Q2
6) DRAIN Q1

MARKING CODE: L02

CMLDM7002AJ*
(Japanese Pinout)



LEAD CODE:
1) SOURCE Q1
2) GATE Q1
3) DRAIN Q2
4) SOURCE Q2
5) GATE Q2
6) DRAIN Q1

MARKING CODE: 02J

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