PROCESS CP210

Small Signal Transistor

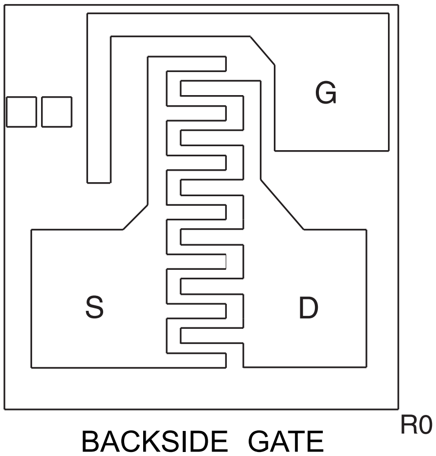
N - Channel Silicon Amplifier J FET Chip

Central™
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	15 x 15 MILS
Die Thickness	8.0 MILS
Drain Bonding Pad Area	3.2 X 4.0 MILS
Source Bonding Pad Area	3.2 X 4.0 MILS
Gate Bonding Pad Area	3.2 X 4.0 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 6,000Å

GEOMETRY



BACKSIDE GATE

GROSS DIE PER 4 INCH WAFER
53,730

PRINCIPAL DEVICE TYPES
2N4416A
CMPF4416A

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R2 (1-August 2002)

PROCESS CP210

Typical Electrical Characteristics

The Typical Electrical Characteristics data
for this chip is currently being revised.

For the latest updated data for this Chip Process,
please visit our website at:

www.centralsemi.com/chip

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