

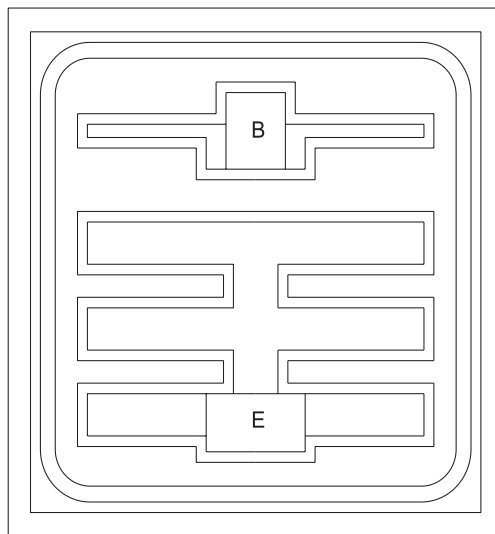
**PROCESS CP221**  
**Small Signal Transistor**  
NPN- High Voltage Darlington Transistor Chip

**Central**<sup>TM</sup>  
**Semiconductor Corp.**

**PROCESS DETAILS**

Process	EPITAXIAL BASE
Die Size	39.5 X 39.5 MILS
Die Thickness	9.8 MILS
Base Bonding Pad Area	3.9 x 5.1 MILS
Emitter Bonding Pad Area	7.9 x 3.9 MILS
Top Side Metalization	Al - 24,000Å
Back Side Metalization	Au - 12,000Å

**GEOMETRY**



BACKSIDE COLLECTOR

R0

**GROSS DIE PER 4 INCH WAFER**

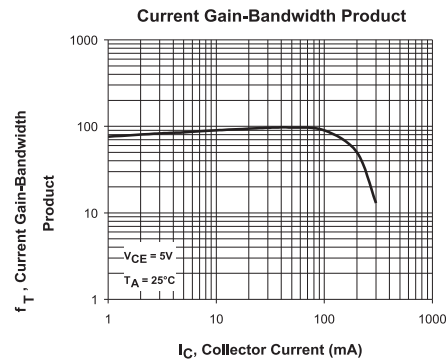
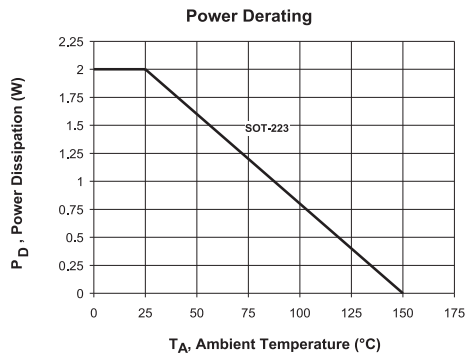
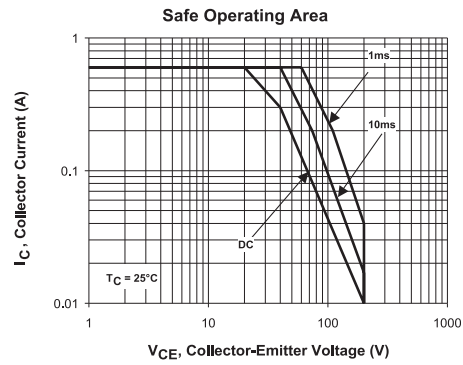
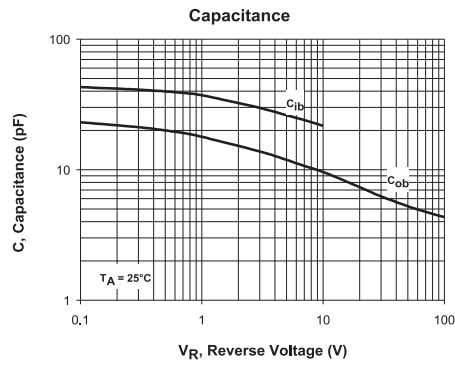
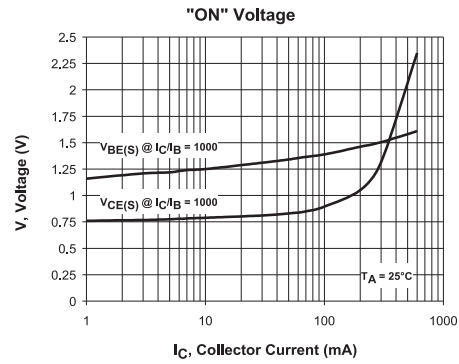
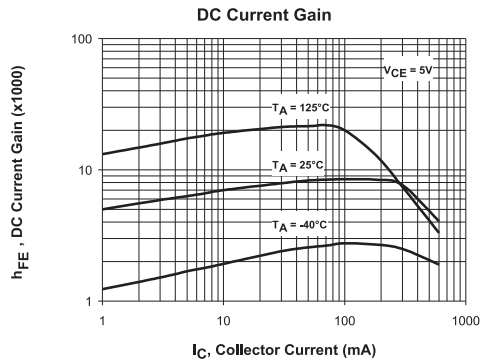
7,290

**PRINCIPAL DEVICE TYPES**

CZT2000

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