PROCESS CP324

Small Signal MOSFET Transistor

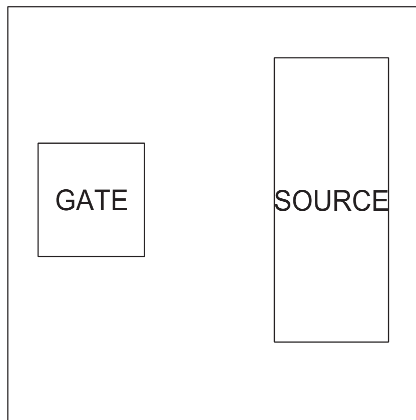
N-Channel Enhancement-Mode Transistor Chip

Central™
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	21.65 x 21.65 MILS
Die Thickness	9.0 MILS
Gate Bonding Pad Area	5.5 x 5.5 MILS
Source Bonding Pad Area	5.9 x 13.8 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 12,000Å

GEOMETRY



BACKSIDE DRAIN R0

GROSS DIE PER 5 INCH WAFER
35,900

PRINCIPAL DEVICE TYPES
2N7002

145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

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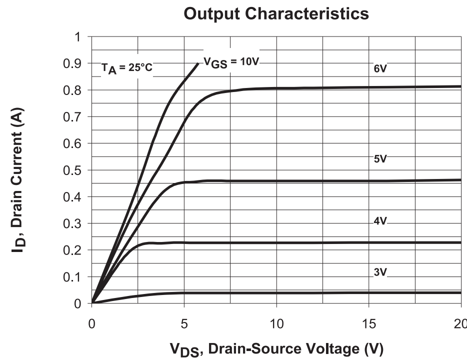
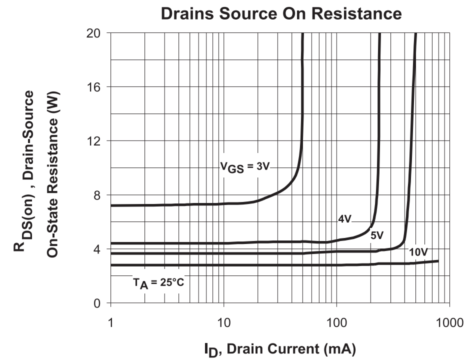
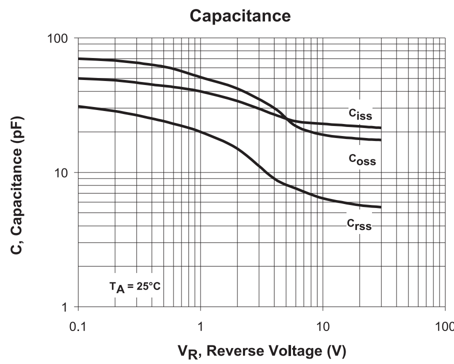
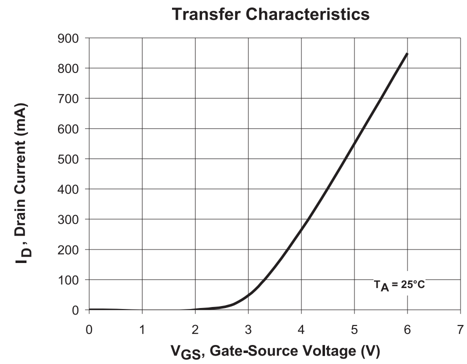
PROCESS CP324

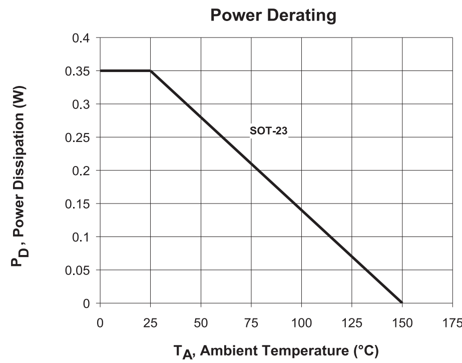
Typical Electrical Characteristics











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