PROCESS CP555

Small Signal Transistor

PNP - Saturated Switch Transistor Chip

Central™ Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	15 X 10 MILS
Die Thickness	8 MILS
Base Bonding Pad Area	3.6 X 2.4 MILS
Emitter Bonding Pad Area	3.6 X 2.4 MILS
Top Side Metalization	Al - 20,000Å
Back Side Metalization	Au - 15,000Å

GEOMETRY

BACKSIDE COLLECTOR

R0

GROSS DIE PER 4 INCH WAFER

75,330

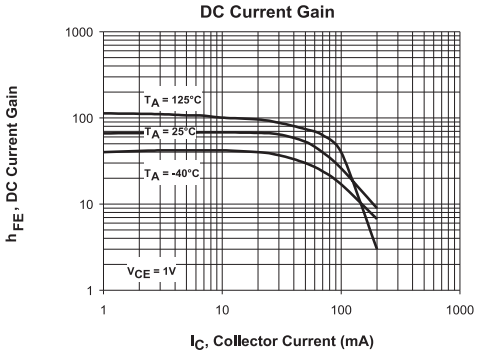
PRINCIPAL DEVICE TYPES

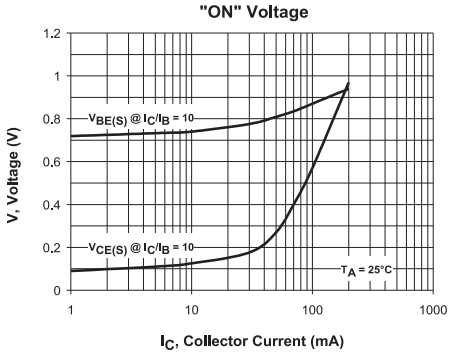
CMPT3640
CMPT4209
2N4209

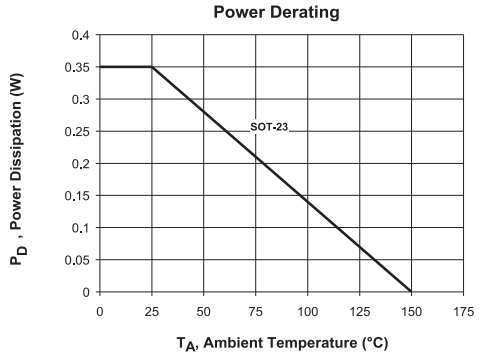
145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

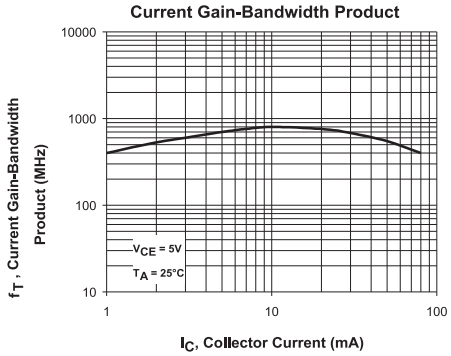
R2 (1-August 2002)

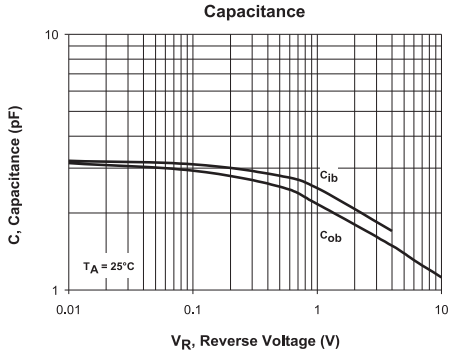
Typical Electrical Characteristics











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