

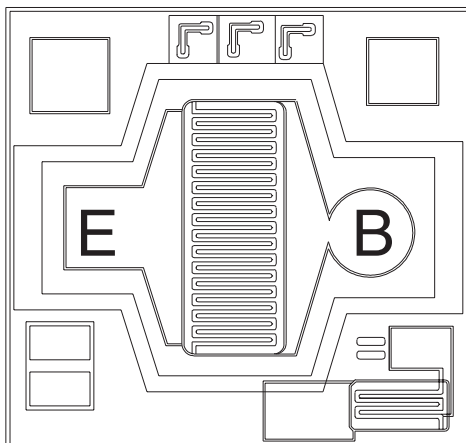
PROCESS CP618
Small Signal Transistor
PNP - Silicon RF Transistor Chip

CentralTM
Semiconductor Corp.

PROCESS DETAILS

| | |
|--------------------------|-------------------|
| Process | EPITAXIAL PLANAR |
| Die Size | 21.7 x 21.7 MILS |
| Die Thickness | 9.0 MILS |
| Base Bonding Pad Area | 3.5 MILS DIAMETER |
| Emitter Bonding Pad Area | 3.5 x 3.5 MILS |
| Top Side Metalization | Al - 30,000Å |
| Back Side Metalization | Au - 10,000Å |

GEOMETRY



R0

BACKSIDE COLLECTOR

GROSS DIE PER 4 INCH WAFER

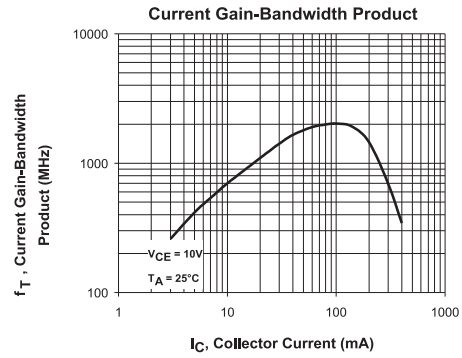
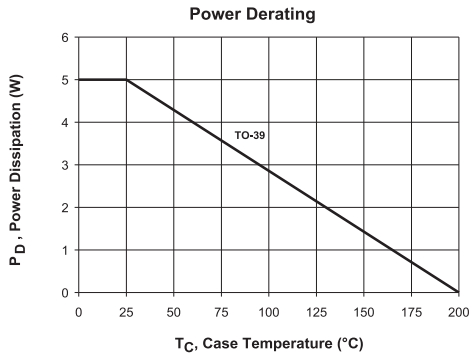
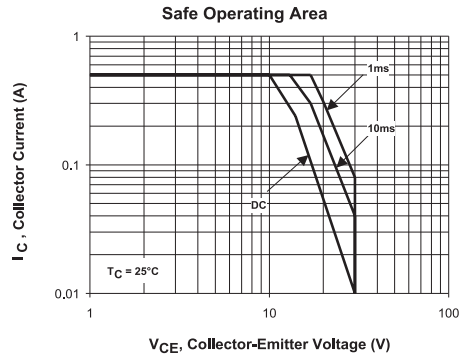
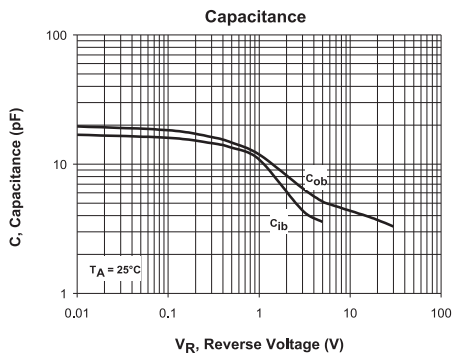
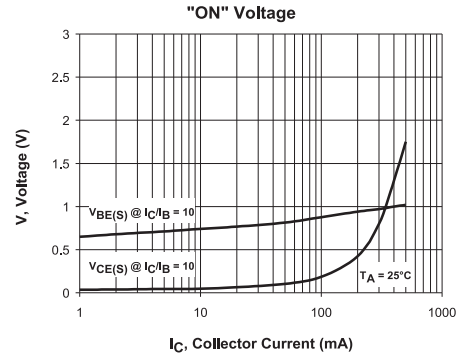
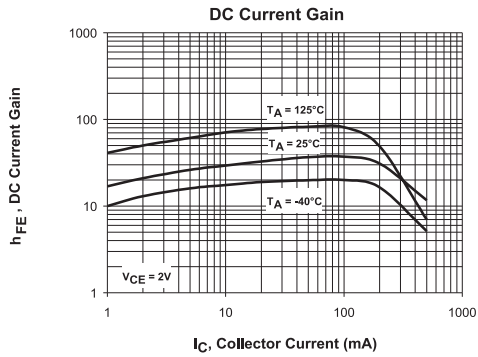
23,990

PRINCIPAL DEVICE TYPES

CM5583

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R2 (1-August 2002)



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