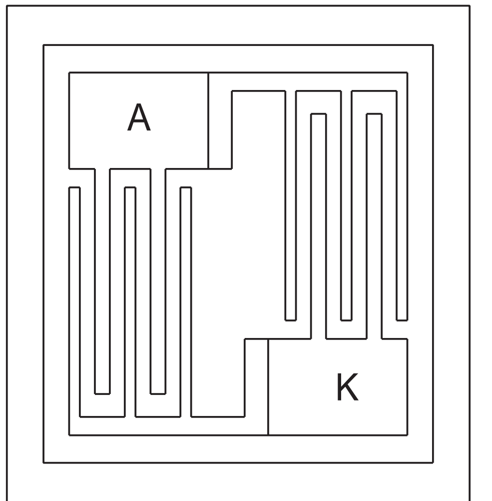
Central™
Semiconductor Corp.

PROCESS CP624
Programmable Unijunction Transistor

PROCESS DETAILS

Process	PLANAR PASSIVATED
Die Size	27.5 x 27.5 MILS
Die Thickness	11 MILS
Anode Bonding Pad Area	7.1 x 5.1 MILS
Cathode Bonding Pad Area	7.1 x 5.1 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 13,000Å

GEOMETRY



BACKSIDE GATE

GROSS DIE PER 4 INCH WAFER
14,930

PRINCIPAL DEVICE TYPES
2N6028

The Typical Electrical Characteristics data for this chip is currently being revised.

For the latest updated data for this Chip Process, please visit our website at:

www.centralsemi.com/chip

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