PROCESS CP712

Power Transistor

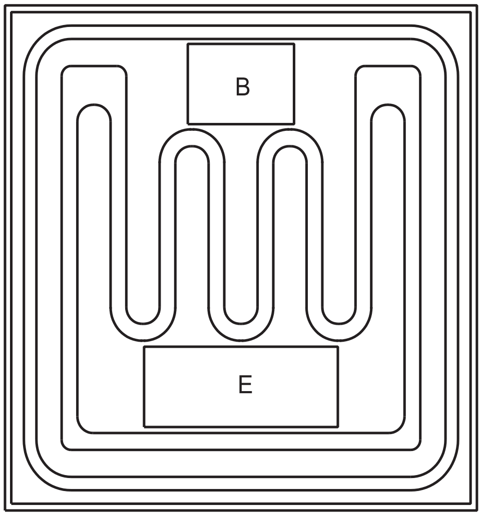
PNP - Amp/Switch Transistor Chip

Central™
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	75 x 75 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	17 x 12 MILS
Emitter Bonding Pad Area	31 x 12 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Ti/Ni/Ag - 11,300Å

GEOMETRY



BACKSIDE COLLECTOR R0

GROSS DIE PER 4 INCH WAFER
1,960

PRINCIPAL DEVICE TYPES
CZT7120

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R1 (1-August 2002)

PROCESS CP712

Typical Electrical Characteristics

The Typical Electrical Characteristics data
for this chip is currently being revised.

For the latest updated data for this Chip Process,
please visit our website at:

www.centralsemi.com/chip

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