N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD16323Q3C

FEATURES

- **DualCool™ Package**
- **Optimized for 5V Gate Drive**
- **Ultra Low Q_g and Q_{gd}**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 3.3-mm × 3.3-mm Plastic Package**

APPLICATIONS

- **Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems**
- **Optimized for Control or Synchronous FET Applications**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion and optimized for 5V gate drive applications.

PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25		V
Q_g	Gate Charge Total (4.5V)	6.2		nC
Q_{gd}	Gate Charge Gate to Drain	1.1		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3V	5.4	mΩ
		V_{GS} = 4.5V	4.4	mΩ
		V_{GS} = 8V	3.8	mΩ
V_{th}	Threshold Voltage	1.1		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16323Q3C	SON 3.3-mm × 3.3-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

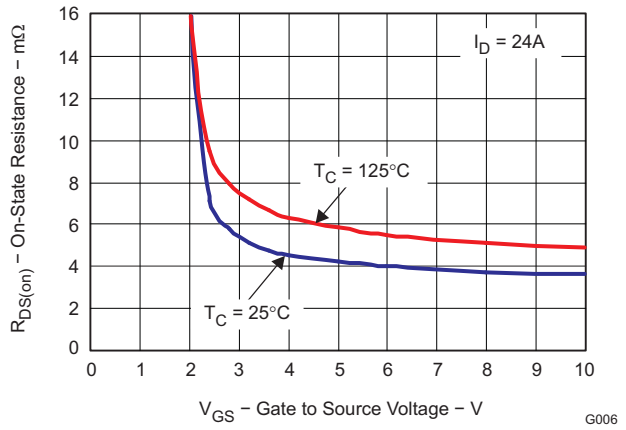
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+10 / –8	V
I_D	Continuous Drain Current, T_C = 25°C	60	A
	Continuous Drain Current(1)	21	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	112	A
P_D	Power Dissipation(1)	3	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 50A, L = 0.1mH, R_G = 25Ω	125	mJ

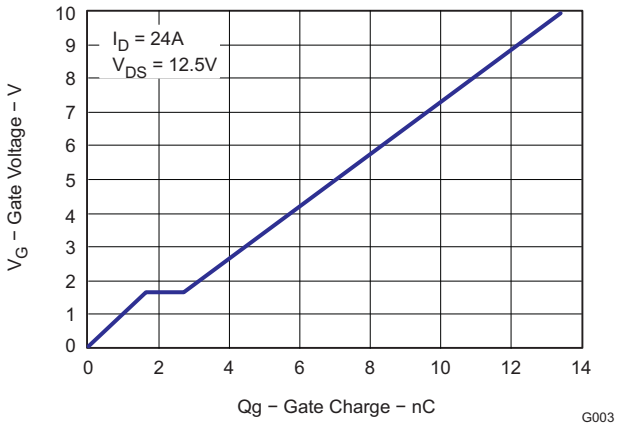
(1) Typical $R_{\theta JA}$ = 43°C/W when mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤300μs, duty cycle ≤2%

$R_{DS(ON)}$ vs V_{GS}



GATE CHARGE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

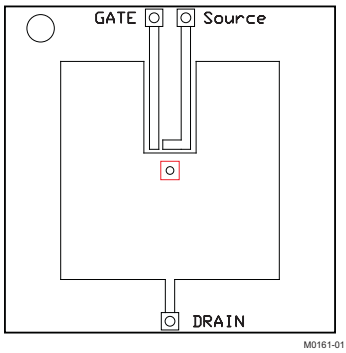
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250µA	25			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 20V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +10/-8V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3V, I_D = 24A		5.4	7.2	mΩ
		V_{GS} = 4.5V, I_D = 24A		4.4	5.5	mΩ
		V_{GS} = 8V, I_D = 24A		3.8	4.5	mΩ
g_{fs}	Transconductance	V_{DS} = 12.5V, I_D = 24A		108		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz		1020	1300	pF
C_{OSS}	Output Capacitance			740	960	pF
C_{RSS}	Reverse Transfer Capacitance			50	65	pF
R_g	Series Gate Resistance			1.4	2.8	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 12.5V, I_D = 24A		6.2	8.4	nC
Q_{gd}	Gate Charge Gate to Drain			1.1		nC
Q_{gs}	Gate Charge Gate to Source			1.8		nC
Qg(th)	Gate Charge at Vth			1		nC
Q_{OSS}	Output Charge	V_{DS} = 12.5V, V_{GS} = 0V		14		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5V, V_{GS} = 4.5V I_D = 24A R_G = 2Ω		5.3		ns
t_r	Rise Time			15		ns
$t_{d(off)}$	Turn Off Delay Time			13		ns
t_f	Fall Time			6.3		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = 24A, V_{GS} = 0V		0.85	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 12.5V, I_F = 24A, di/dt = 300A/µs		21		nC
t_{rr}	Reverse Recovery Time	V_{DD} = 12.5V, I_F = 24A, di/dt = 300A/µs		16		ns

THERMAL CHARACTERISTICS

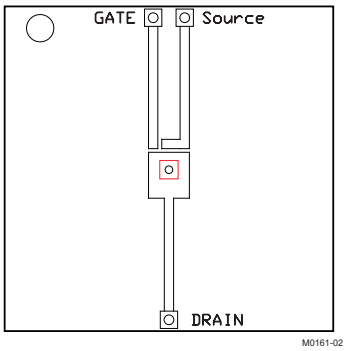
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$\theta_{JC(top)}$	Junction-to-case (top) thermal resistance			3.5	°C/W
$\theta_{JC(bot)}$	Junction-to-case (bottom) thermal resistance (1)			2.7	°C/W
θ_{JA}	Junction to Ambient thermal resistance (1) (2)			58	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 58°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 162°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

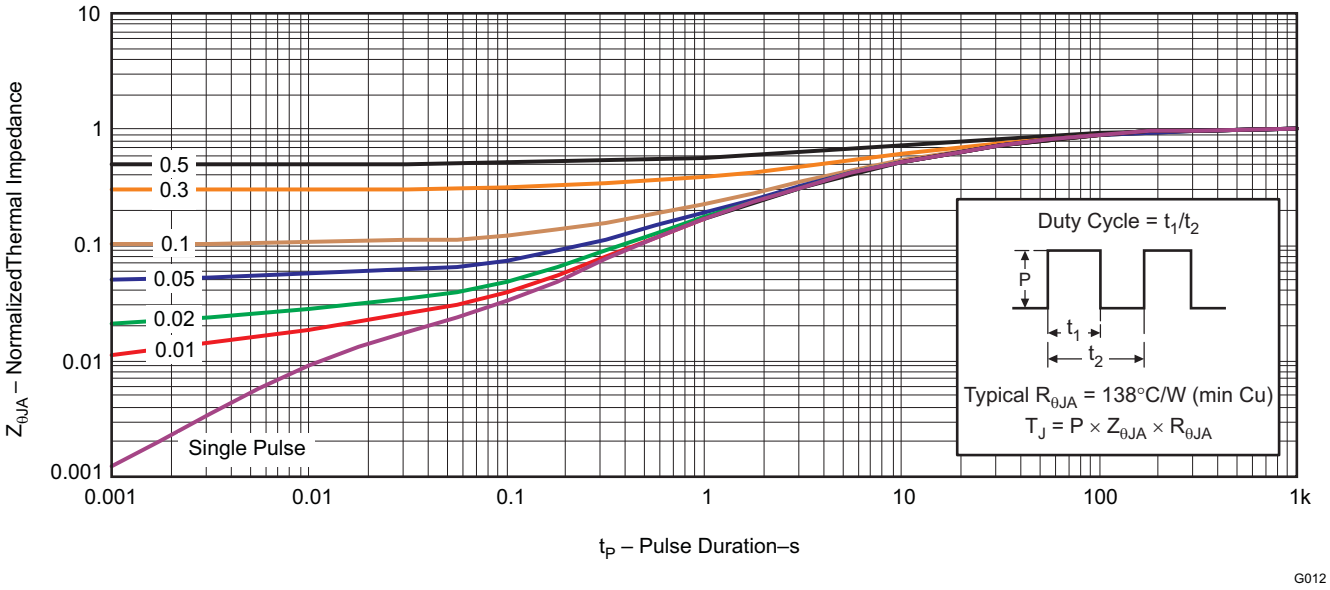


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

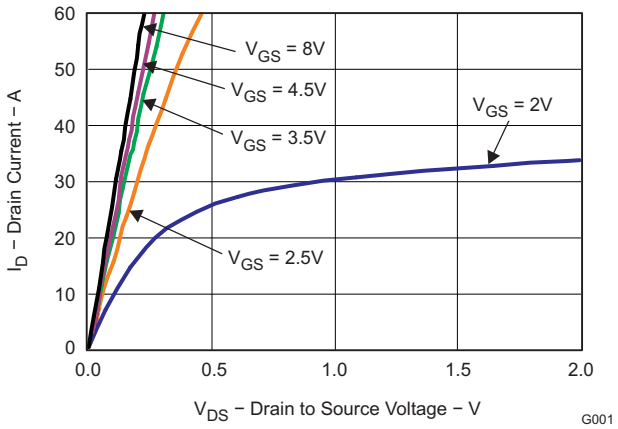


Figure 2. Saturation Characteristics

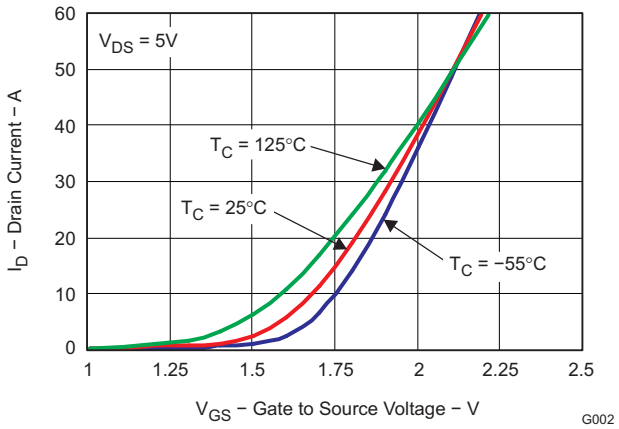


Figure 3. Transfer Characteristics

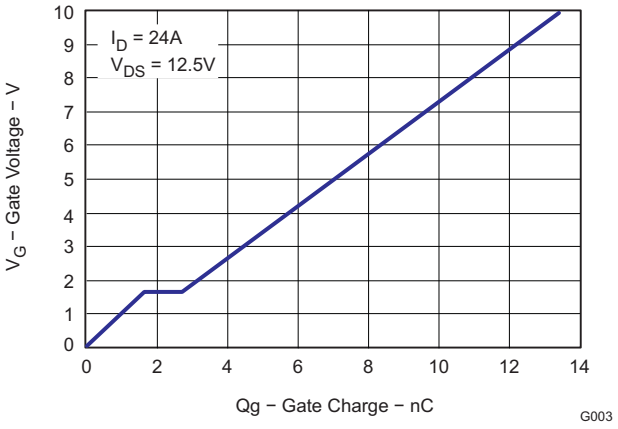


Figure 4. Gate Charge

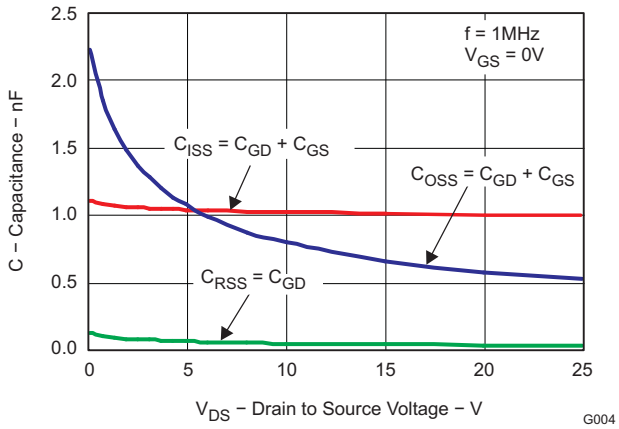


Figure 5. Capacitance

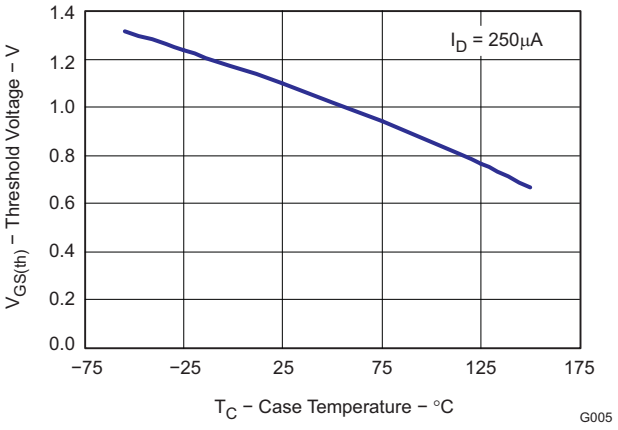


Figure 6. Threshold Voltage vs. Temperature

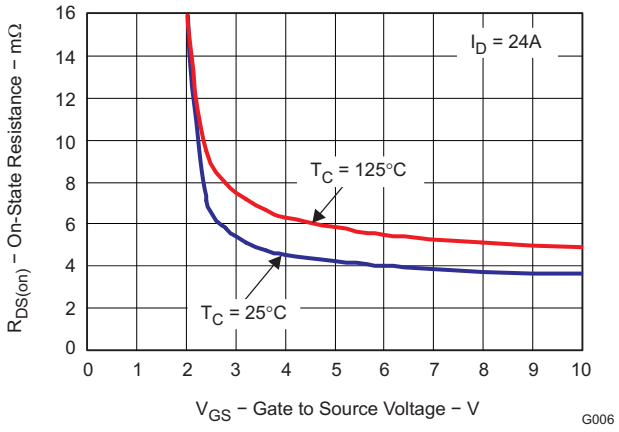


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

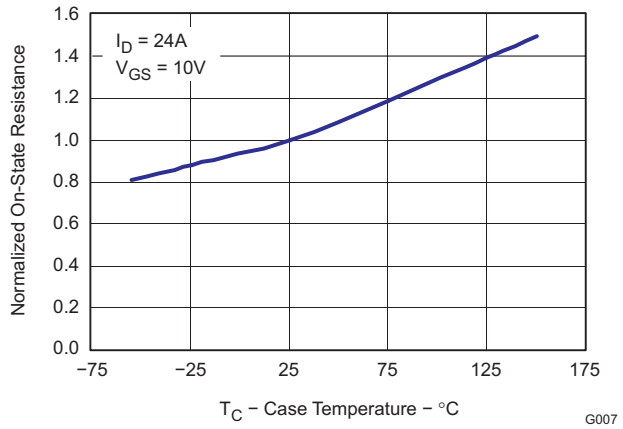


Figure 8. Normalized On-State Resistance vs. Temperature

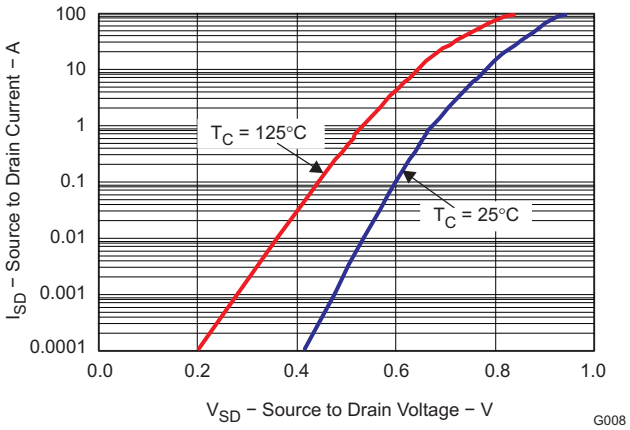


Figure 9. Typical Diode Forward Voltage

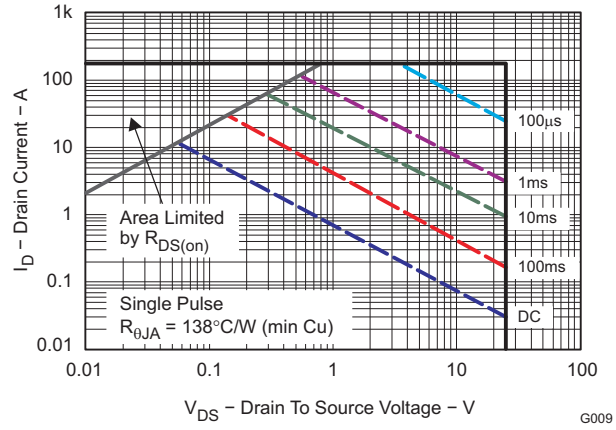


Figure 10. Maximum Safe Operating Area

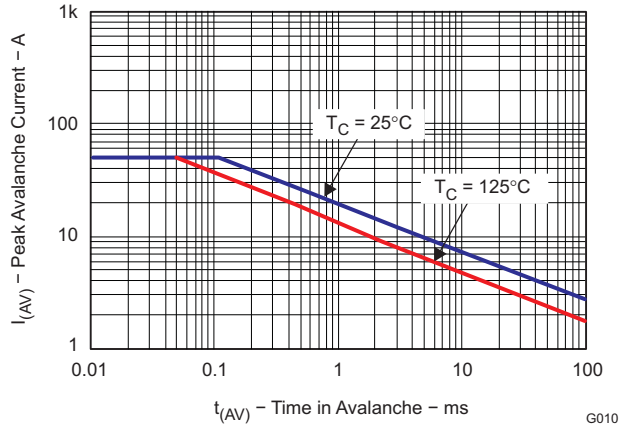


Figure 11. Single Pulse Unclamped Inductive Switching

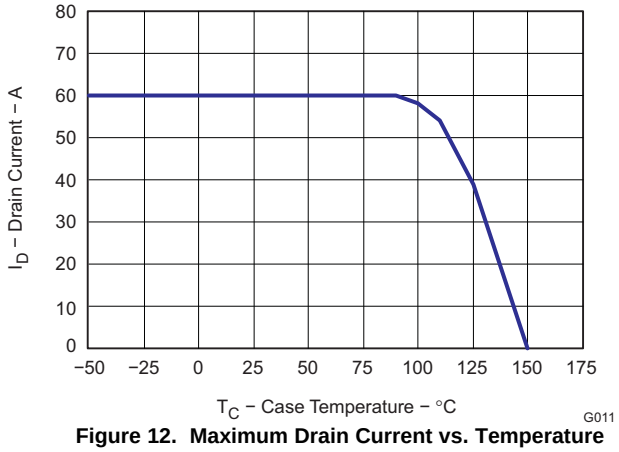
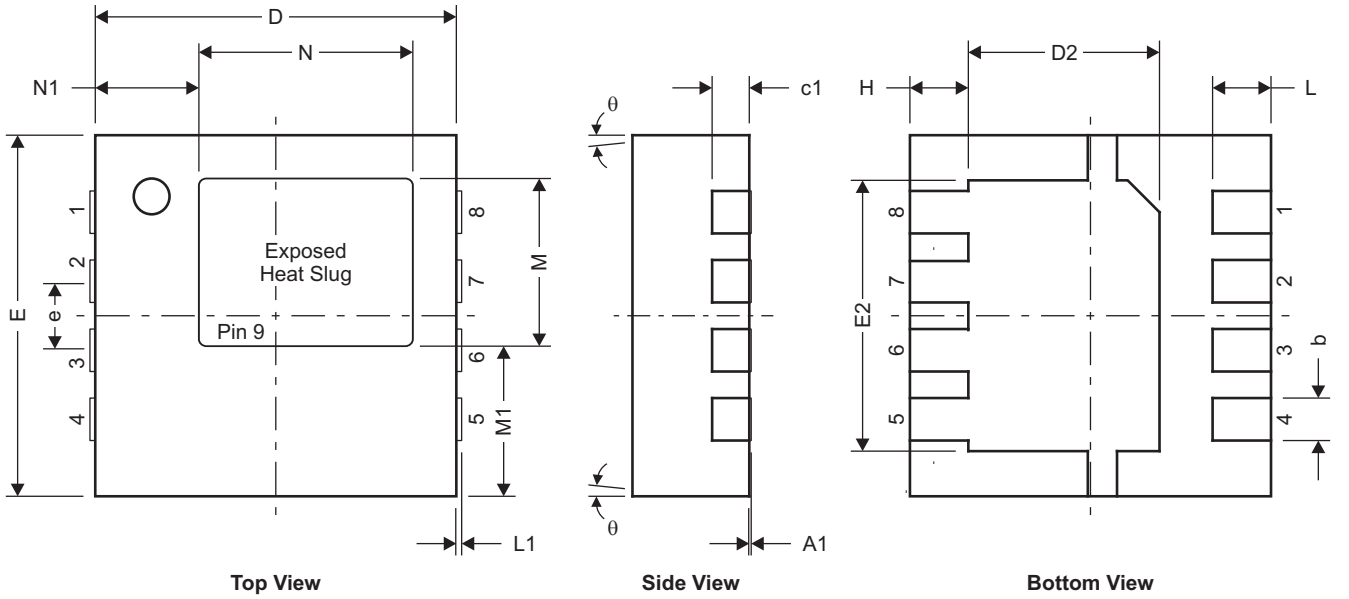


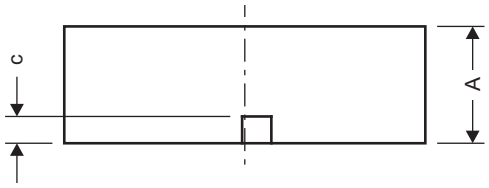
Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q3C Package Dimensions



Top View **Side View** **Bottom View**



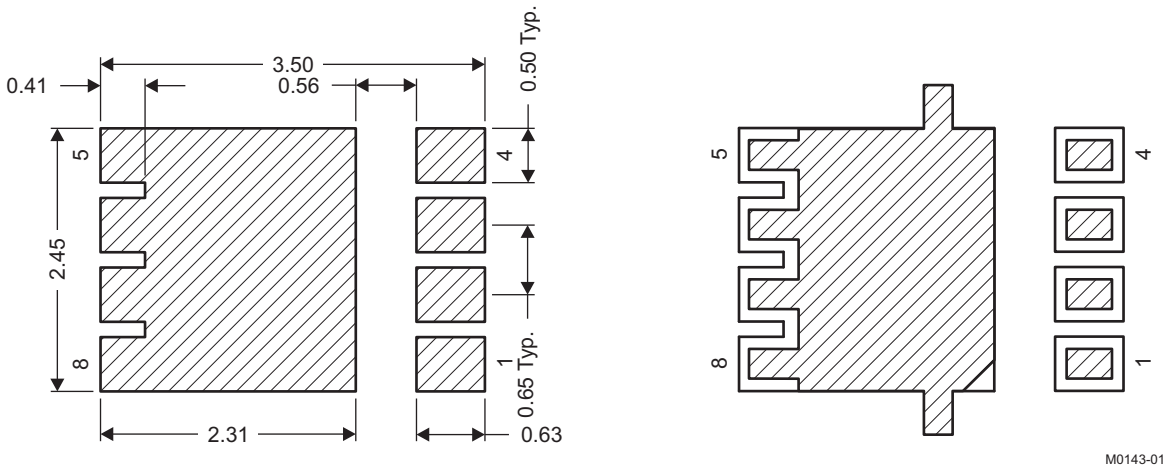
Front View

Pinout	
Pin #	**Label**
1, 2, 3, 9	Source
4	Gate
5, 6, 7, 8	Drain

M0198-01

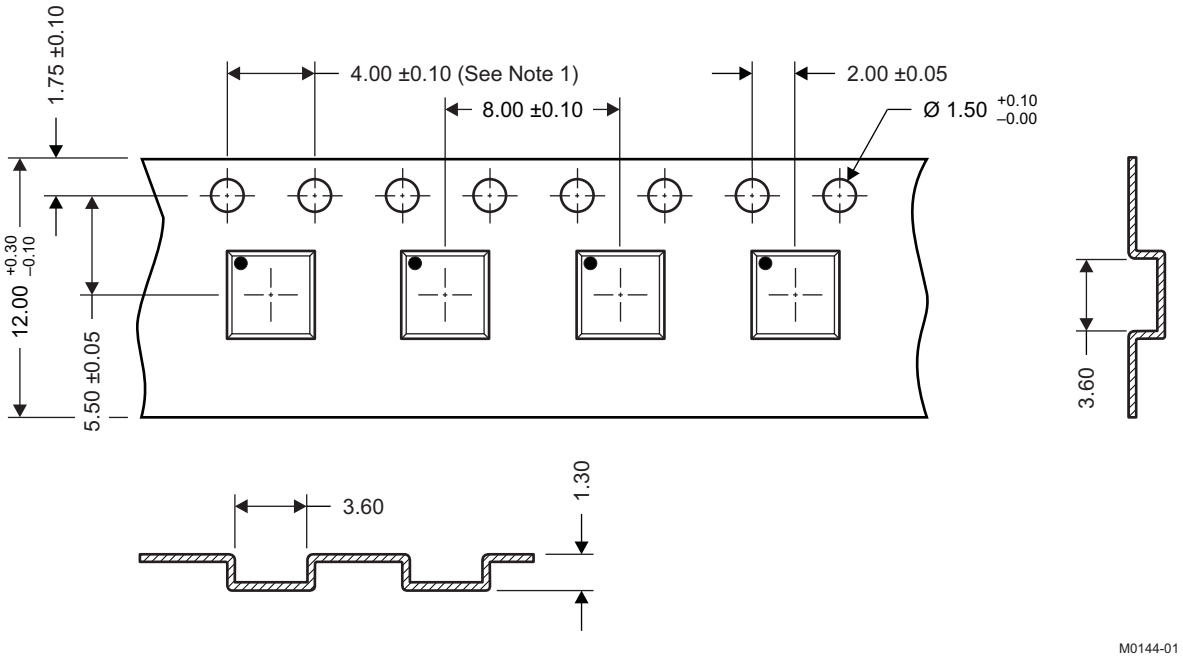
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
c	0.150	0.200	0.250	0.006	0.008	0.010
c1	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	–	–	–	–	–	–
M	1.561	1.661	1.761	0.061	0.065	0.069
M1	1.130	1.230	1.330	0.044	0.048	0.052
N	1.854	1.954	2.054	0.073	0.077	0.081
N1	0.846	0.946	1.046	0.033	0.037	0.041
θ	–	–	–	–	–	–

Recommended PCB Pattern



For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

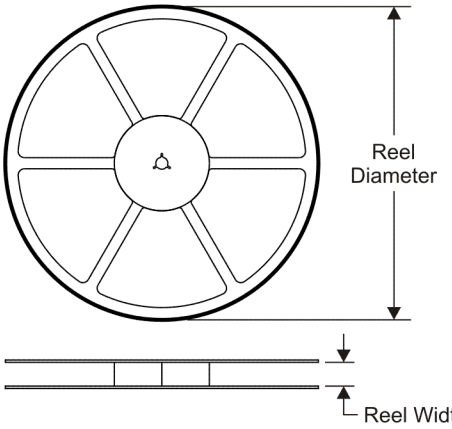
Q3 Tape and Reel Information



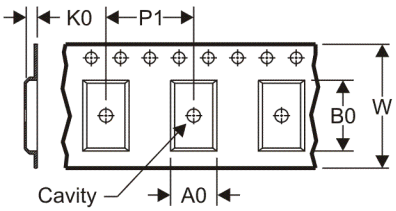
NOTES: 1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm, unless otherwise specified.
5. Thickness: 0.30 ±0.05mm
6. MSL1 260°C (IR and convection) PbF reflow compatible

TAPE AND REEL INFORMATION

REEL DIMENSIONS

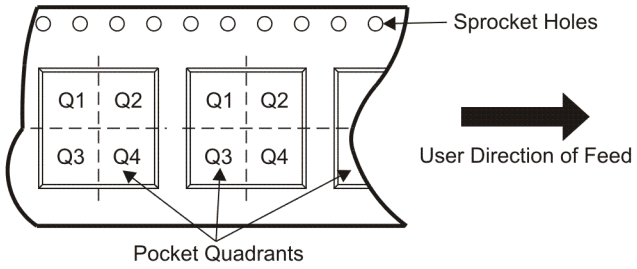


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

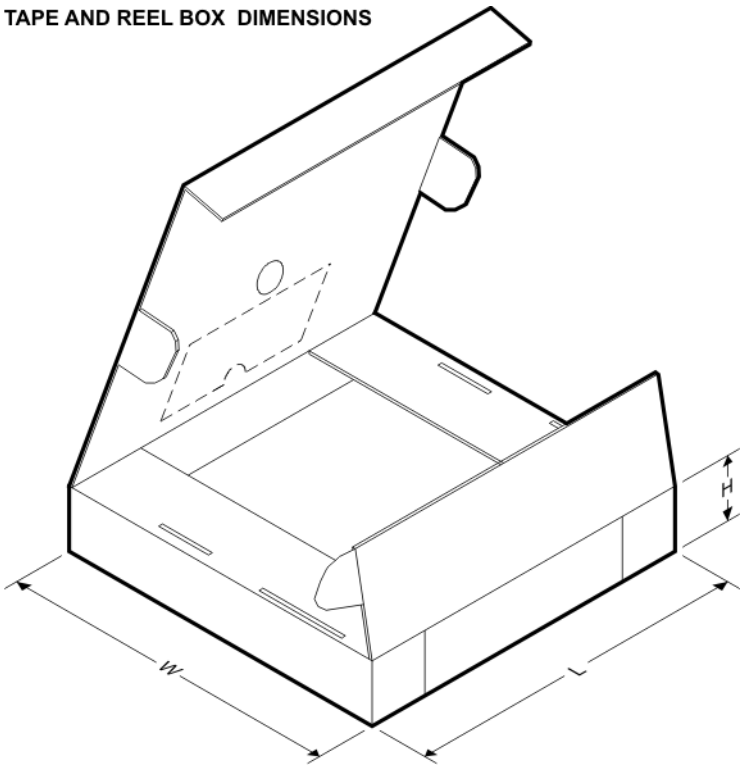
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16323Q3C	SON	DQV	8	2500	330.0	12.8	3.6	3.6	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16323Q3C	SON	DQV	8	2500	335.0	335.0	32.0

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