DTC114EXV3T1 Series

Digital Transistors (BRT)

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The digital transistor contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. The digital transistor eliminates these individual components by integrating them into a single device. The use of a digital transistor can reduce both system cost and board space. The device is housed in the SC−89 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch/3000 Unit Tape & Reel
- Lead−Free Solder Plating (Pure Sn)

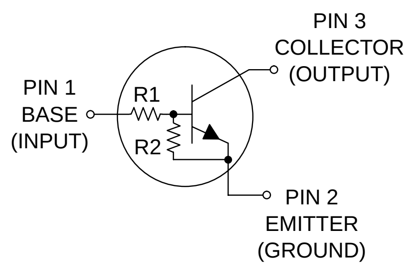
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

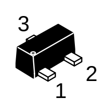
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

ON Semiconductor®

http://onsemi.com

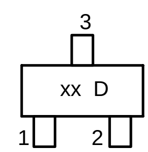
NPN SILICON DIGITAL TRANSISTORS





SC−89
CASE 463C
STYLE 1

MARKING DIAGRAM



xx = Specific Device Code
(See Marking Table on page 2)
D = Date Code

© Semiconductor Components Industries, LLC, 2004

January, 2004 − Rev. 0
Publication Order Number:
DTC114EXV3T1/D

DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Shipping†
DTC114EXV3T1	8A	10	10	3000/Tape & Reel
DTC124EXV3T1	8B	22	22	
DTC144EXV3T1	8C	47	47	
DTC114YXV3T1	8D	10	47	
DTC114TXV3T1	94	10	∞	
DTC143TXV3T1	8F	4.7	∞	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation, FR−4 Board (Note 1) @ T_A = 25°C Derate above 25°C	P_D	 200 1.6	 mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	600	°C/W
Total Device Dissipation, FR−4 Board (Note 2) @ T_A = 25°C Derate above 25°C	P_D	 300 2.4	 mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	400	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

1. FR−4 @ Minimum Pad.
2. FR−4 @ 1.0 × 1.0 Inch Pad.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	–	–	100	nAdc
Collector−Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	–	–	500	nAdc
Emitter−Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	DTC114EXV3T1	I_{EBO}	–	–	0.5	mAdc
	DTC124EXV3T1		–	–	0.2	
	DTC144EXV3T1		–	–	0.1	
	DTC114YXV3T1		–	–	0.2	
	DTC114TXV3T1		–	–	0.9	
	DTC143TXV3T1		–	–	1.9	
Collector−Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	–	–	Vdc
Collector−Emitter Breakdown Voltage (Note 3) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	–	–	Vdc
ON CHARACTERISTICS (Note 3)						
DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA)	DTC114EXV3T1	h_{FE}	35	60	–	
	DTC124EXV3T1		60	100	–	
	DTC144EXV3T1		80	140	–	
	DTC114YXV3T1		80	140	–	
	DTC114TXV3T1		160	350	–	
	DTC143TXV3T1		160	350	–	
Collector−Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA) (I_C = 10 mA, I_B = 1.0 mA)	DTC143TXV3T1/DTC114TXV3T1	$V_{CE(sat)}$	–	–	0.25	Vdc
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	DTC114EXV3T1		–	–	0.2	
	DTC124EXV3T1		–	–	0.2	
	DTC114YXV3T1		–	–	0.2	
	DTC114TXV3T1		–	–	0.2	
	DTC143TXV3T1		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	DTC144EXV3T1		–	–	0.2	
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	DTC143TXV3T1 DTC114TXV3T1	V_{OH}	4.9	–	–	Vdc
Input Resistor	DTC114EXV3T1	R1	7.0	10	13	kΩ
	DTC124EXV3T1		15.4	22	28.6	
	DTC144EXV3T1		32.9	47	61.1	
	DTC114YXV3T1		7.0	10	13	
	DTC114TXV3T1		7.0	10	13	
	DTC143TXV3T1		3.3	4.7	6.1	
Resistor Ratio	DTC114EXV3T1/DTC124EXV3T1/ DTC144EXV3T1	R_1/R_2	0.8	1.0	1.2	
	DTC114YXV3T1		0.17	0.21	0.25	
	DTC143TXV3T1/DTC114TXV3T1		–	–	–	

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.

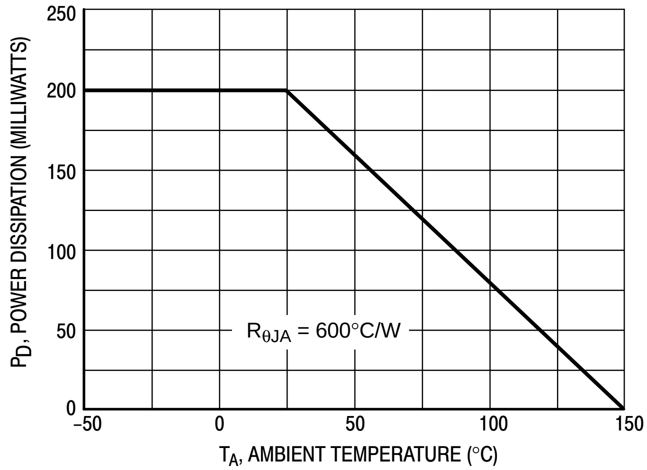


Figure 1. Derating Curve

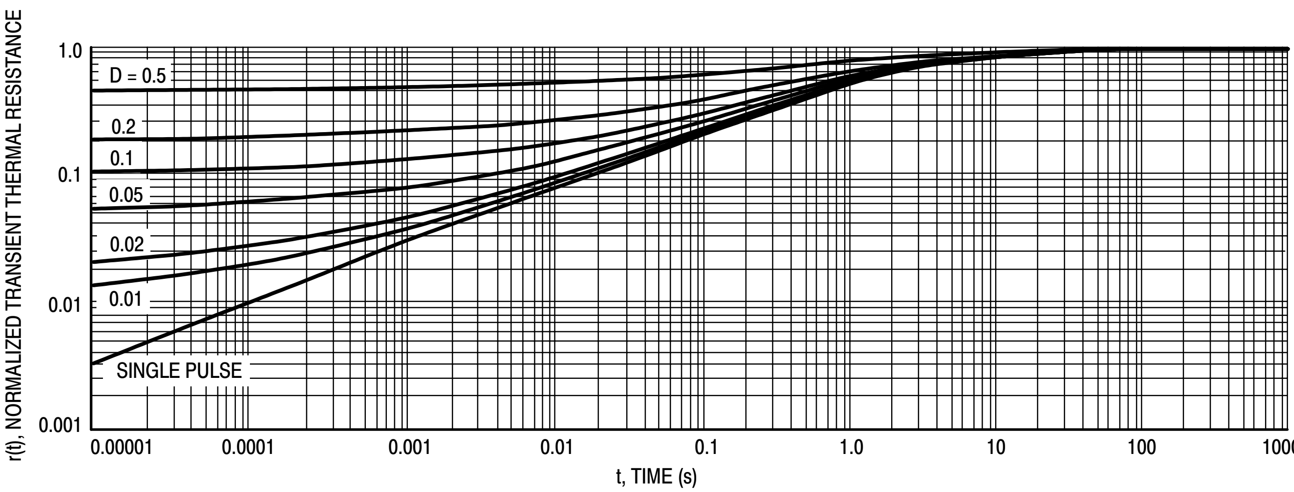


Figure 2. Normalized Thermal Response

TYPICAL ELECTRICAL CHARACTERISTICS − DTC114EXV3T1

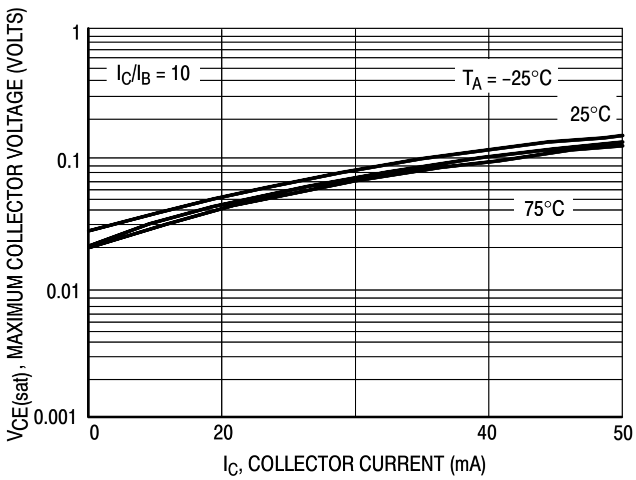


Figure 3. $V_{CE(sat)}$ versus I_C

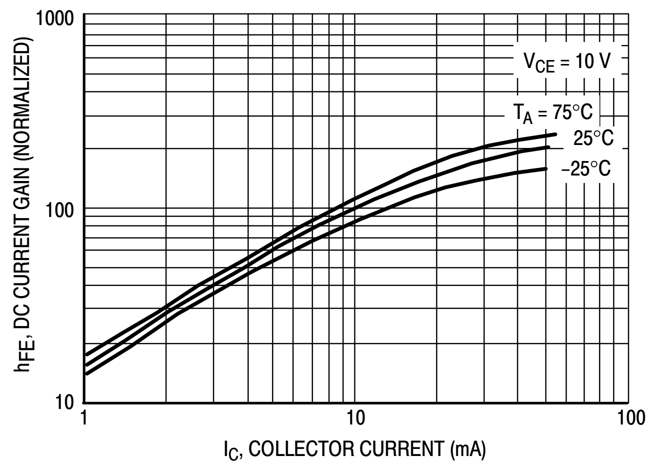


Figure 4. DC Current Gain

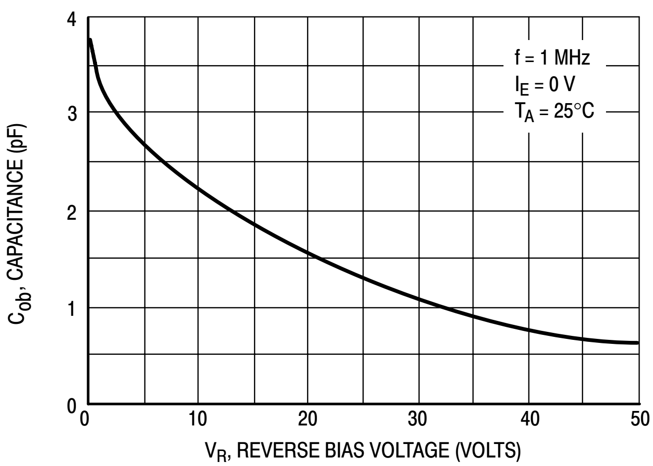


Figure 5. Output Capacitance

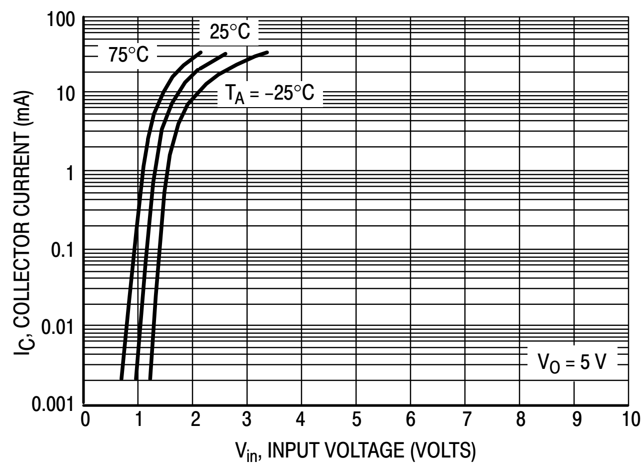


Figure 6. Output Current versus Input Voltage

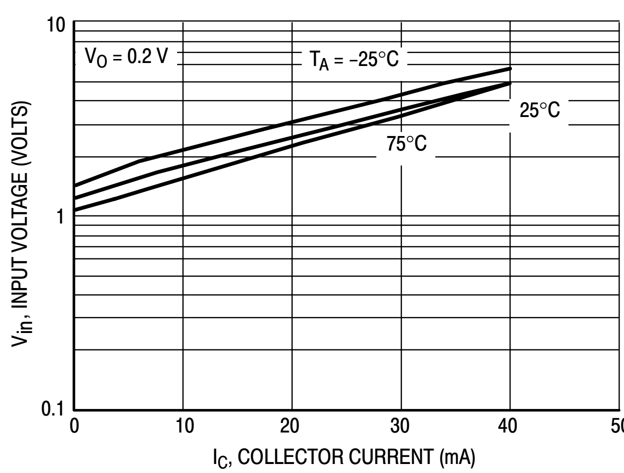


Figure 7. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − DTC124EXV3T1

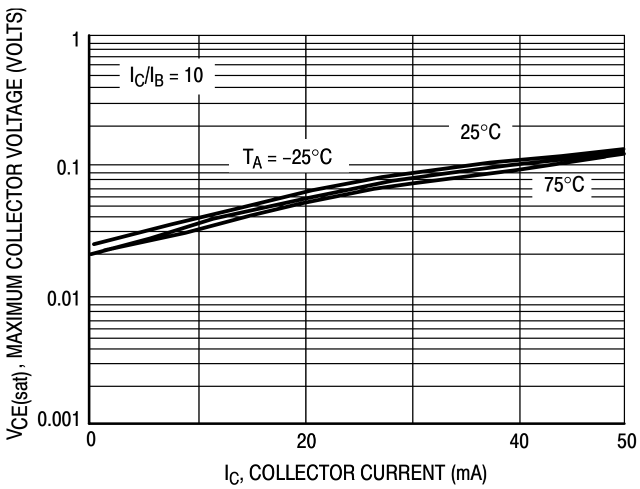


Figure 8. $V_{CE(sat)}$ versus I_C

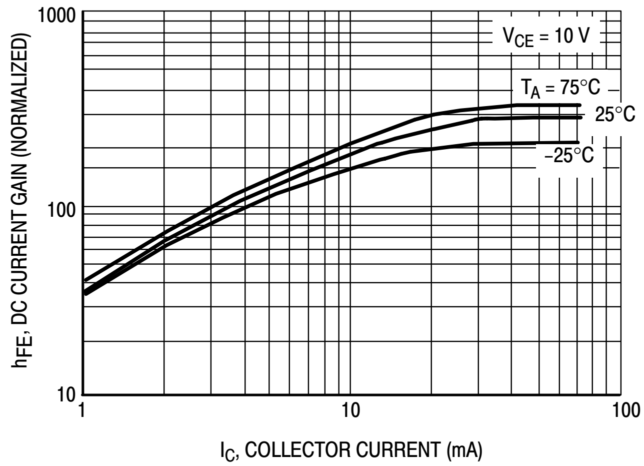


Figure 9. DC Current Gain

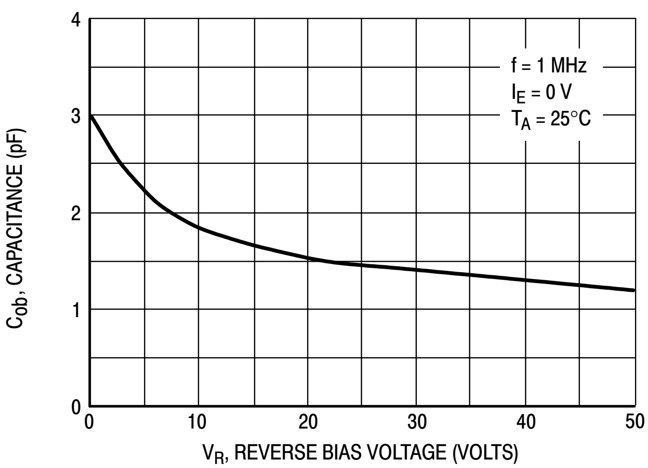


Figure 10. Output Capacitance

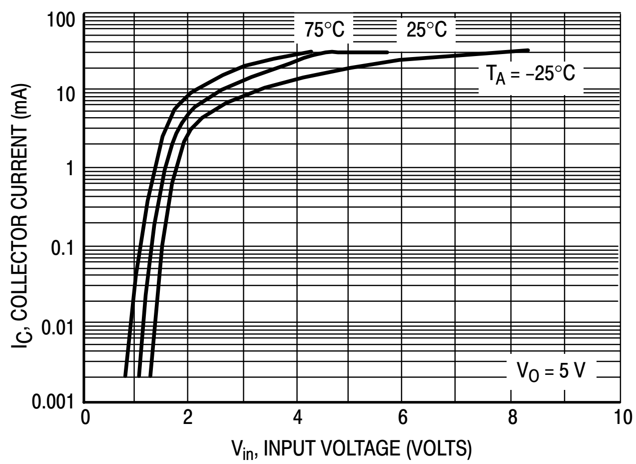


Figure 11. Output Current versus Input Voltage

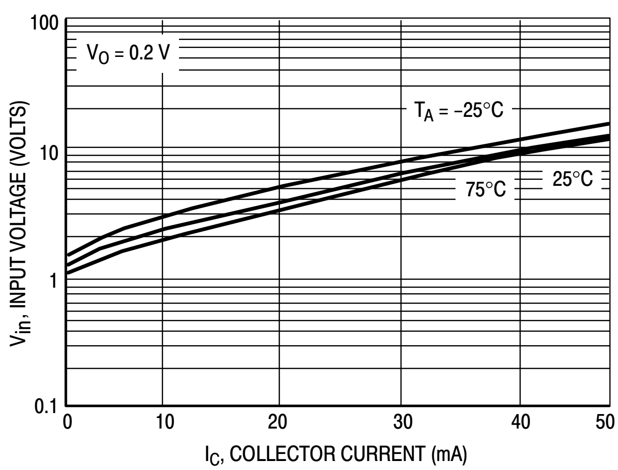


Figure 12. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − DTC144EXV3T1

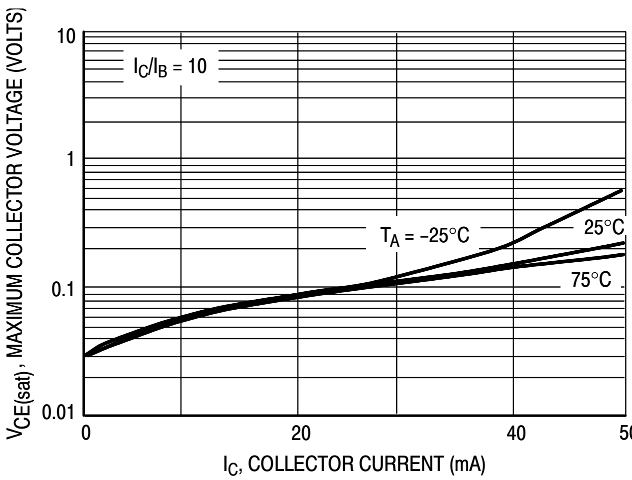


Figure 13. $V_{CE(sat)}$ versus I_C

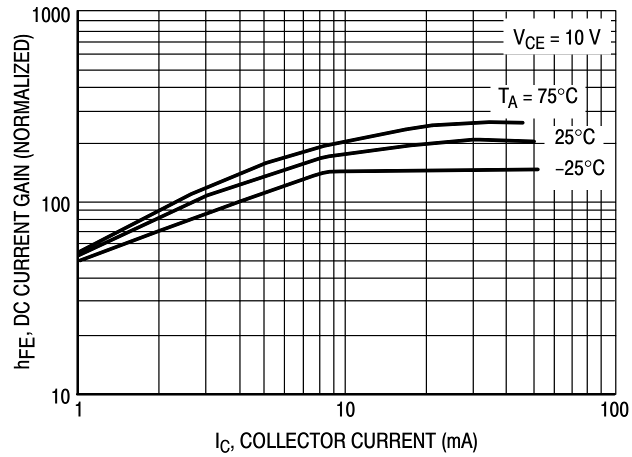


Figure 14. DC Current Gain

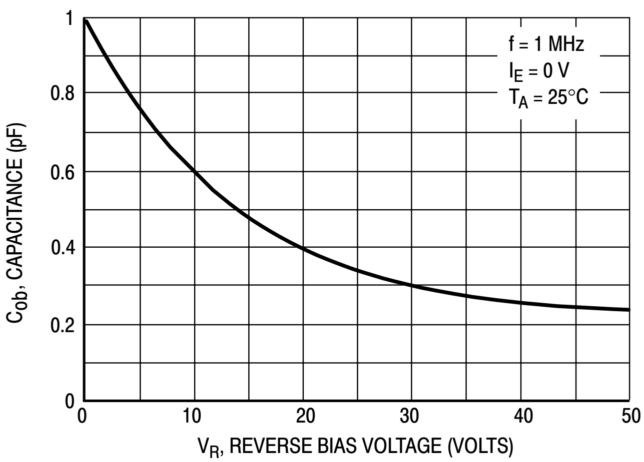


Figure 15. Output Capacitance

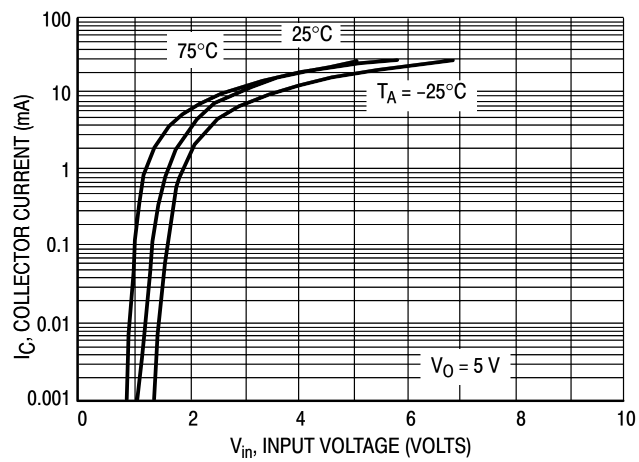


Figure 16. Output Current versus Input Voltage

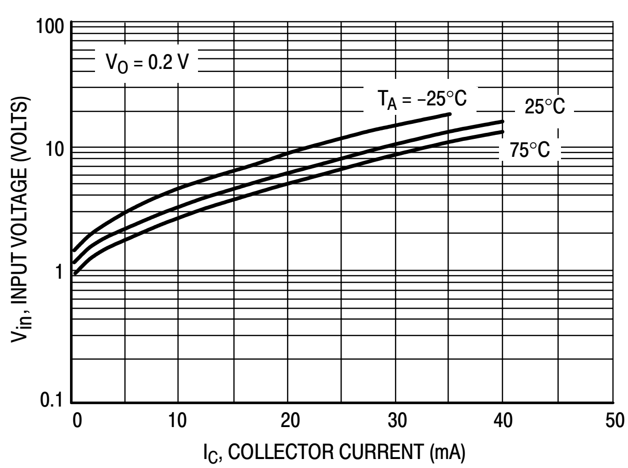


Figure 17. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − DTC114YXV3T1

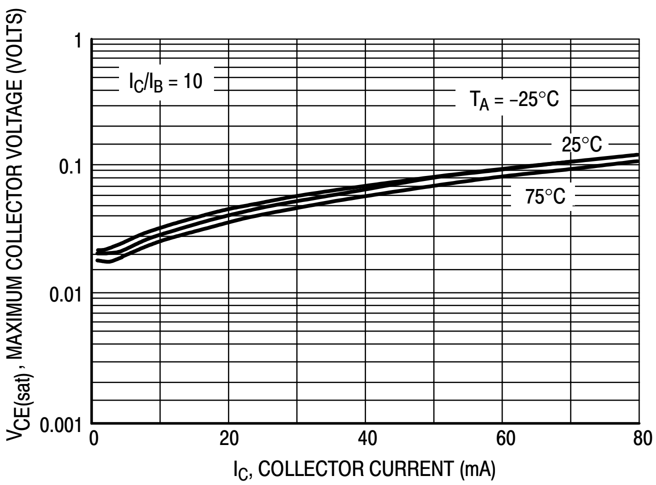


Figure 18. $V_{CE(sat)}$ versus I_C

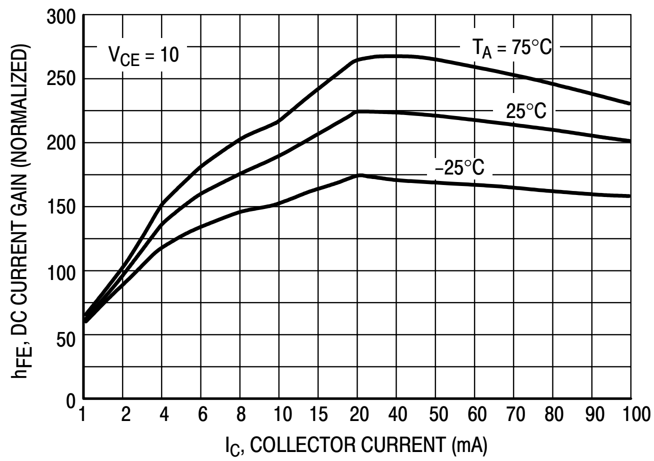


Figure 19. DC Current Gain

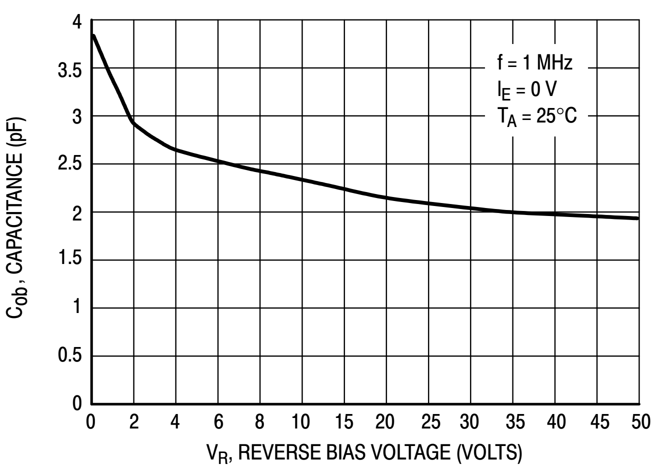


Figure 20. Output Capacitance

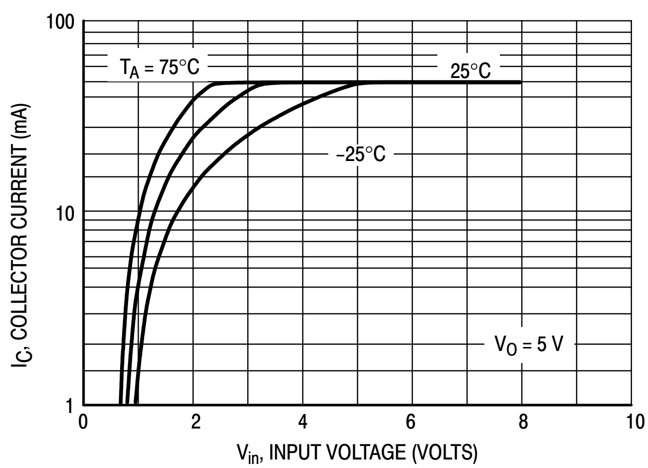


Figure 21. Output Current versus Input Voltage

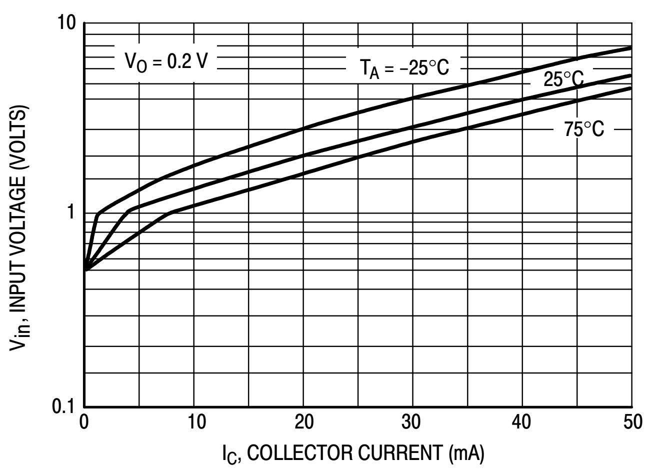


Figure 22. Input Voltage versus Output Current

TYPICAL APPLICATIONS FOR NPN BRTs

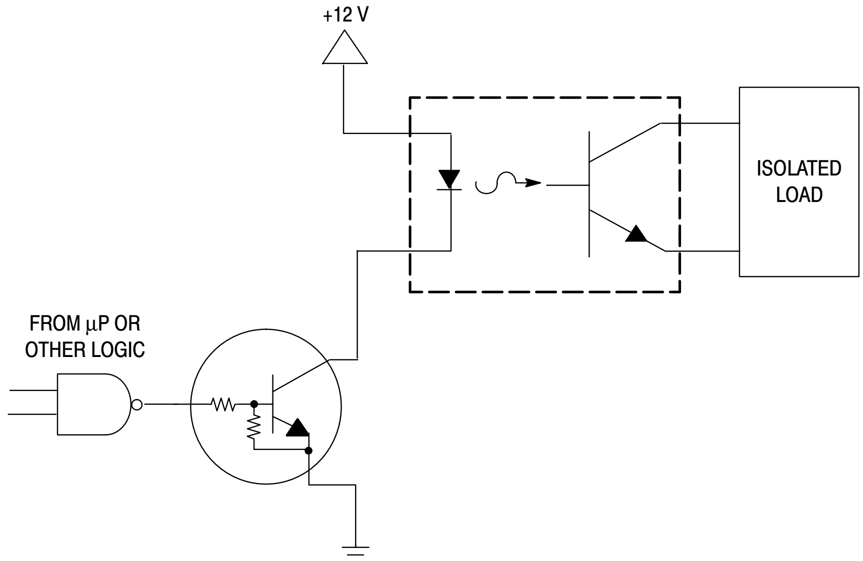


Figure 23. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

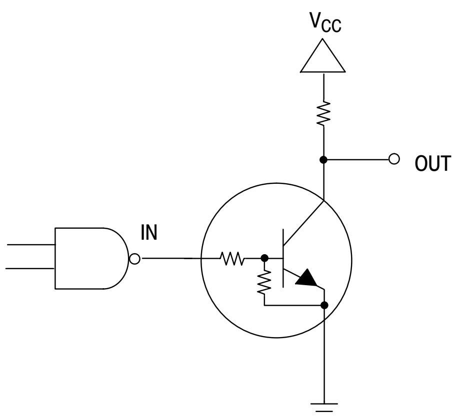


Figure 24. Open Collector Inverter: Inverts the Input Signal

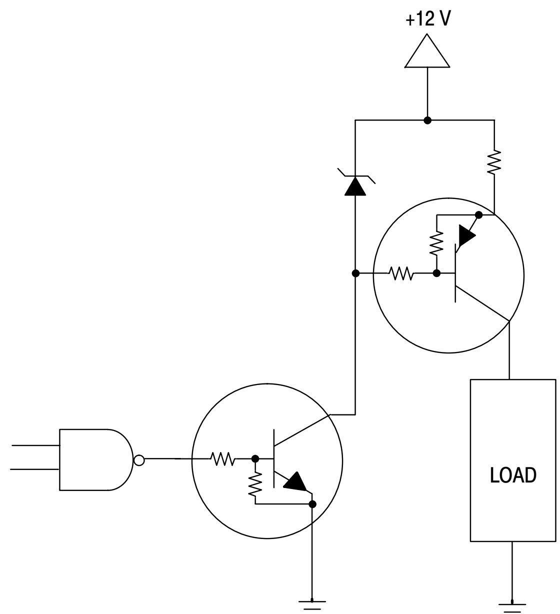
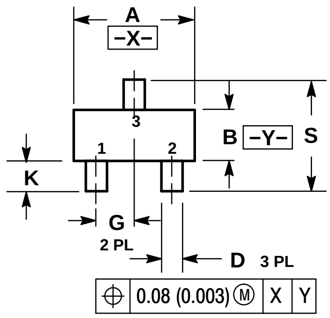
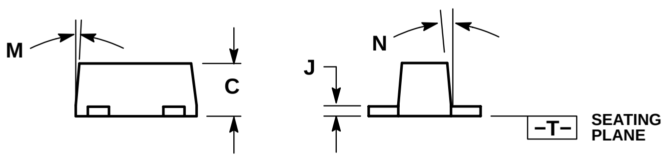


Figure 25. Inexpensive, Unregulated Current Source

PACKAGE DIMENSIONS

SC−89
CASE 463C−03
ISSUE C





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C−01 OBSOLETE, NEW STANDARD 463C−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50 BSC			0.020 BSC		
H	0.53 REF			0.021 REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L	1.10 REF			0.043 REF		
M	−−−	−−−	10	−−−	−−−	10
N	−−−	−−−	10	−−−	−−−	10
S	1.50	1.60	1.70	0.059	0.063	0.067

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.