FAIRCHILD SEMICONDUCTOR®

January 2012

UniFET™

FDB12N50U

N-Channel MOSFET, FRFET

500V, 10A, 0.8Ω

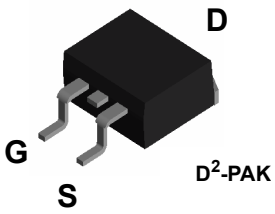
Features

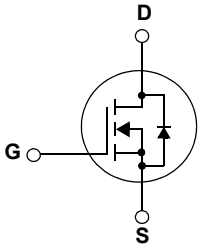
- $R_{DS(on)}$ = 0.65Ω (Typ.)@ V_{GS} = 10V, I_D = 5A
- Low gate charge (Typ. 21nC)
- Low Crss (Typ. 11pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advance technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switching mode power supplies and active power factor correction.





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage		500	V
V_{GSS}	Gate to Source Voltage		±30	V
I_D	Drain Current	-Continuous (T_C = 25°C)	10	A
		-Continuous (T_C = 100°C)	6	
I_{DM}	Drain Current	- Pulsed (Note 1)	40	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	456	mJ
I_{AR}	Avalanche Current	(Note 1)	10	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	16.5	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	20	V/ns
P_D	Power Dissipation	(T_C = 25°C)	165	W
		- Derate above 25°C	1.33	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.75	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

Package Marking and Ordering Information $T_C = 25^oC$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB12N50U	FDB12N50UTM_WS	D2-PAK	330mm	24mm	800

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$, $T_J = 25^oC$	500	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25^oC	-	0.7	-	$V/^oC$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500V$, $V_{GS} = 0V$	-	-	25	μA
		$V_{DS} = 400V$, $T_C = 125^oC$	-	-	250	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30V$, $V_{DS} = 0V$	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 5A$	-	0.65	0.8	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40V$, $I_D = 5A$ (Note 4)	-	11	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz	-	1050	1395	pF
C_{oss}	Output Capacitance		-	140	190	pF
C_{rss}	Reverse Transfer Capacitance		-	11	17	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400V$, $I_D = 10A$, $V_{GS} = 10V$ (Note 4, 5)	-	21	30	nC
Q_{gs}	Gate to Source Gate Charge		-	6	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	9	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250V$, $I_D = 10A$, $R_G = 25\Omega$ (Note 4, 5)	-	35	80	ns
t_r	Turn-On Rise Time		-	45	100	ns
$t_{d(off)}$	Turn-Off Delay Time		-	60	130	ns
t_f	Turn-Off Fall Time		-	35	80	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	10	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	40	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 12A$	-	-	1.6	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 12A$, $dI_F/dt = 100A/\mu s$ (Note 4)	-	60	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.1	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 9mH, $I_{AS} = 10A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25°C$
3. $I_{SD} \le 10A$, $di/dt \le 200A/\mu s$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25°C$
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

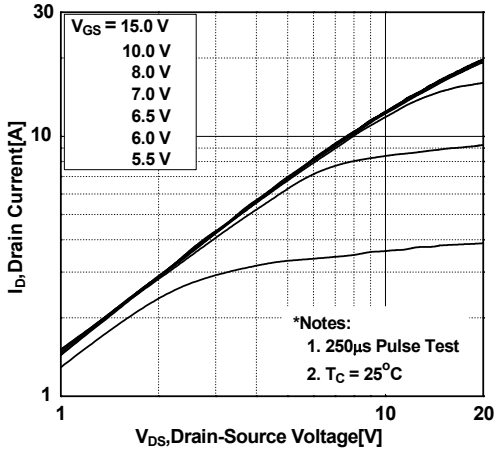


Figure 2. Transfer Characteristics

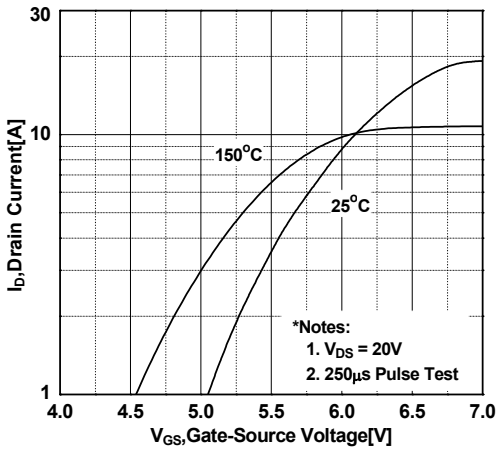


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

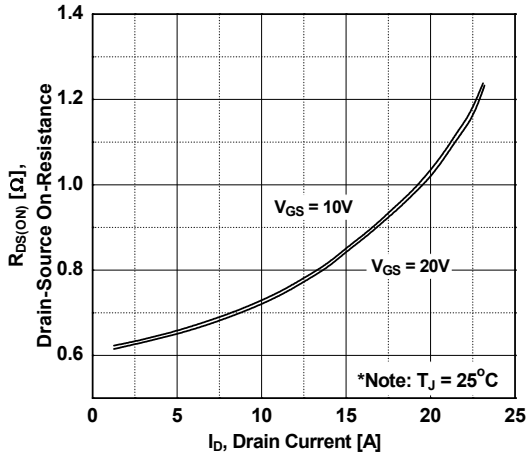


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

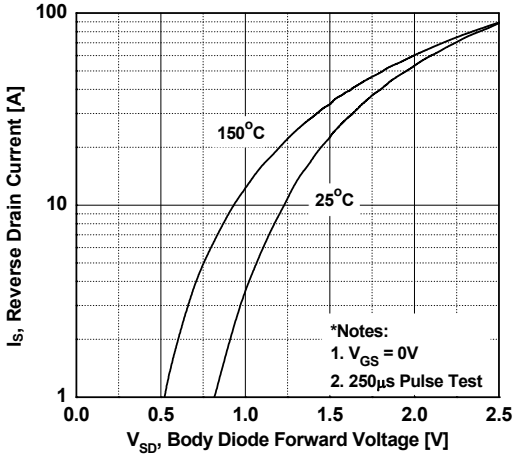


Figure 5. Capacitance Characteristics

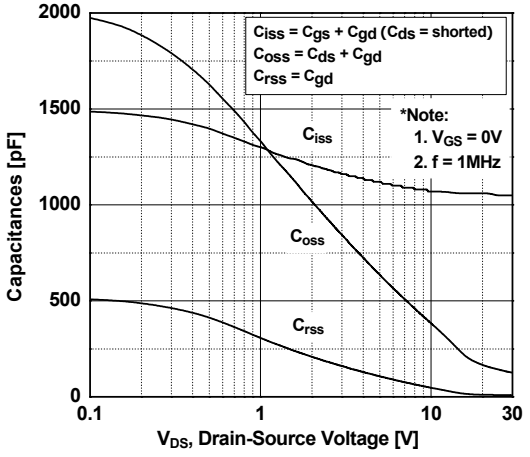
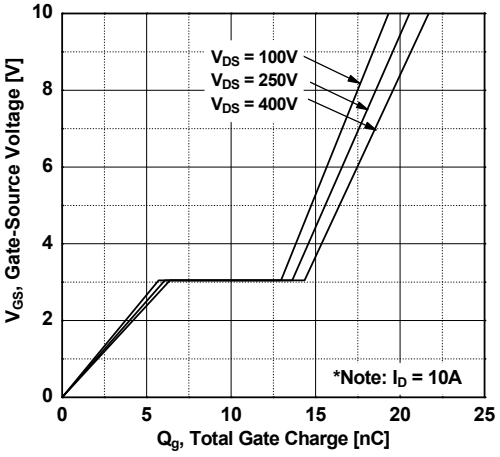


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

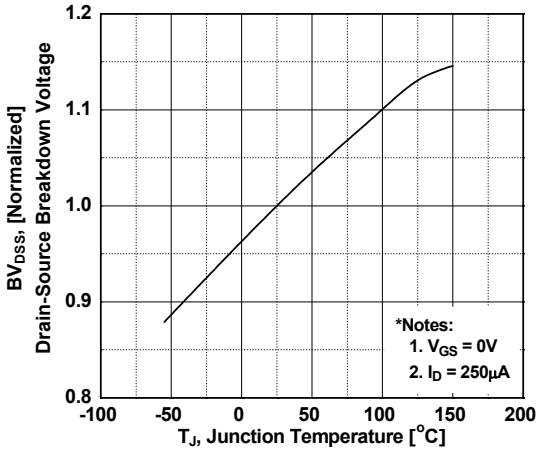


Figure 8. Maximum Safe Operating Area

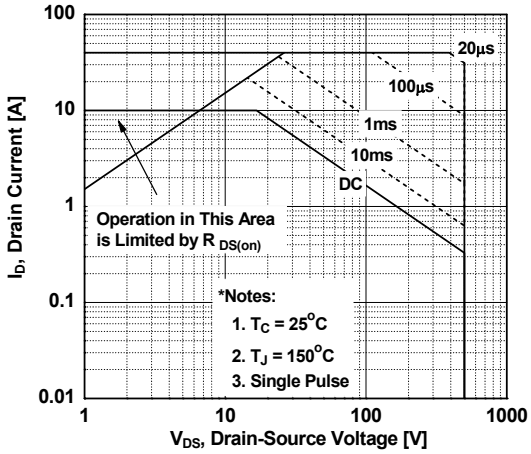


Figure 9. Maximum Drain Current vs. Case Temperature

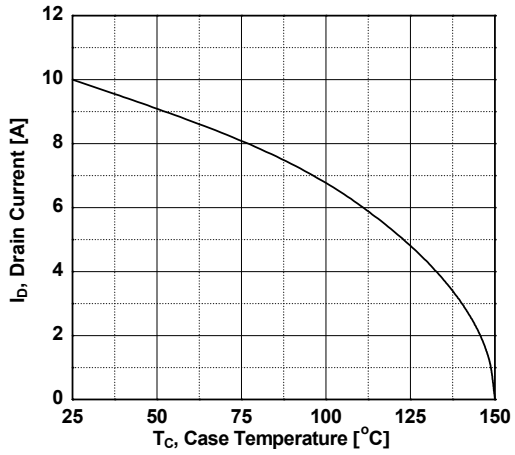
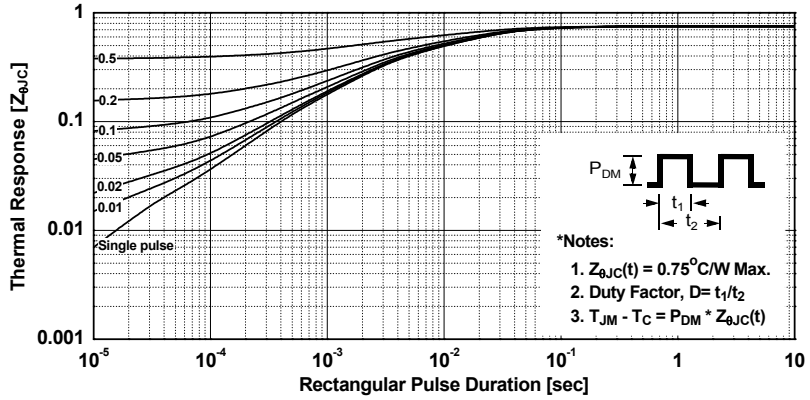
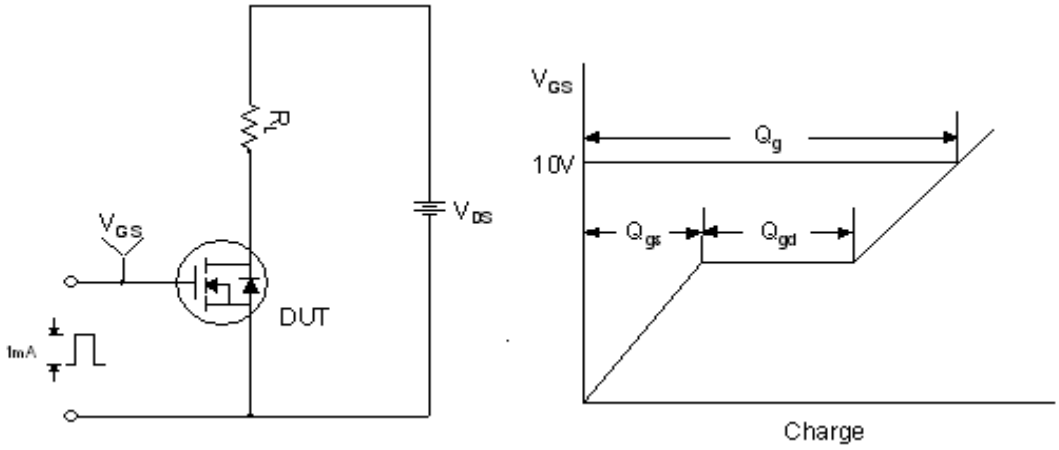


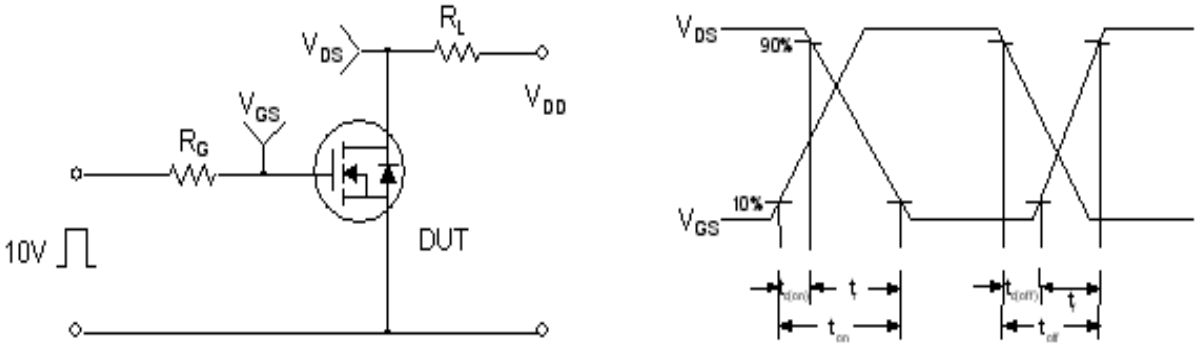
Figure 10. Transient Thermal Response Curve



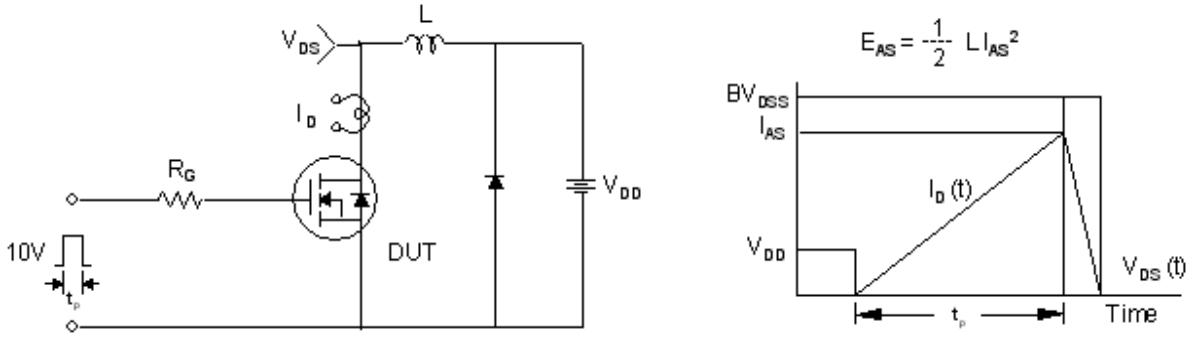
Gate Charge Test Circuit & Waveform



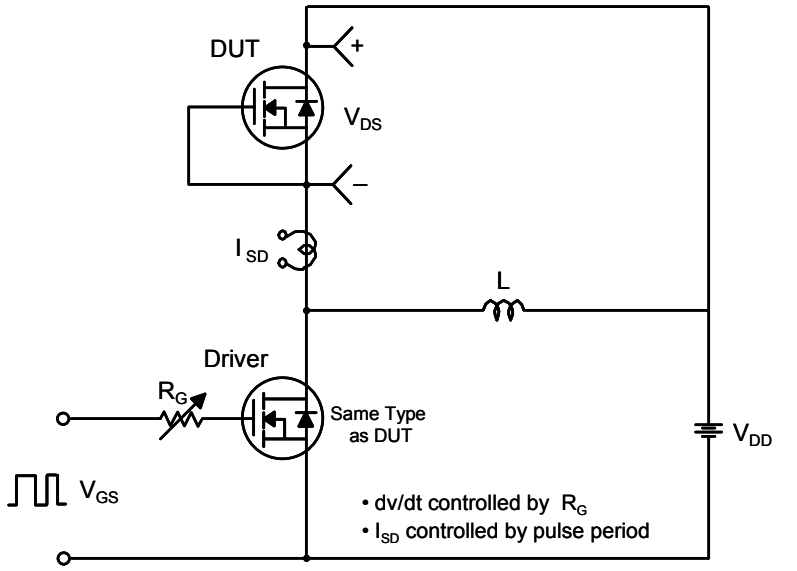
Resistive Switching Test Circuit & Waveforms

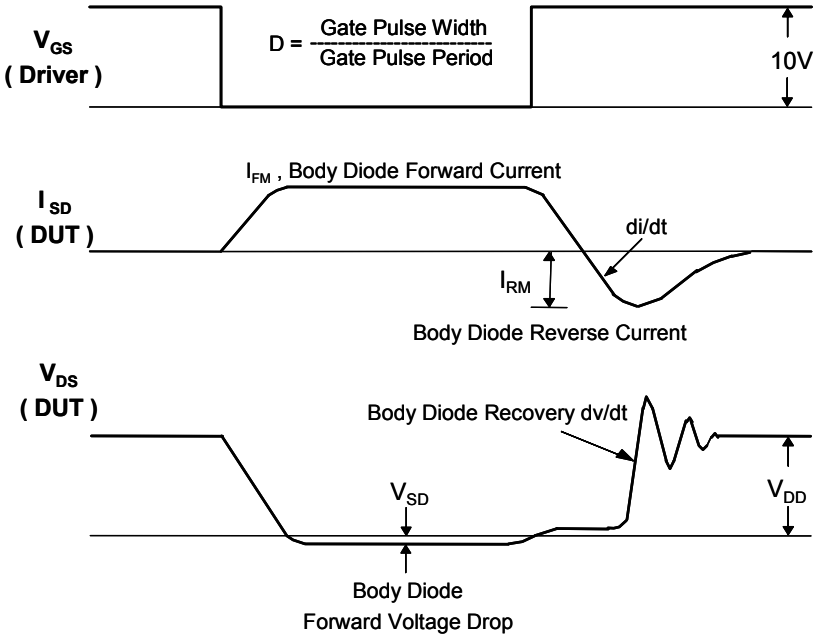


Unclamped Inductive Switching Test Circuit & Waveforms



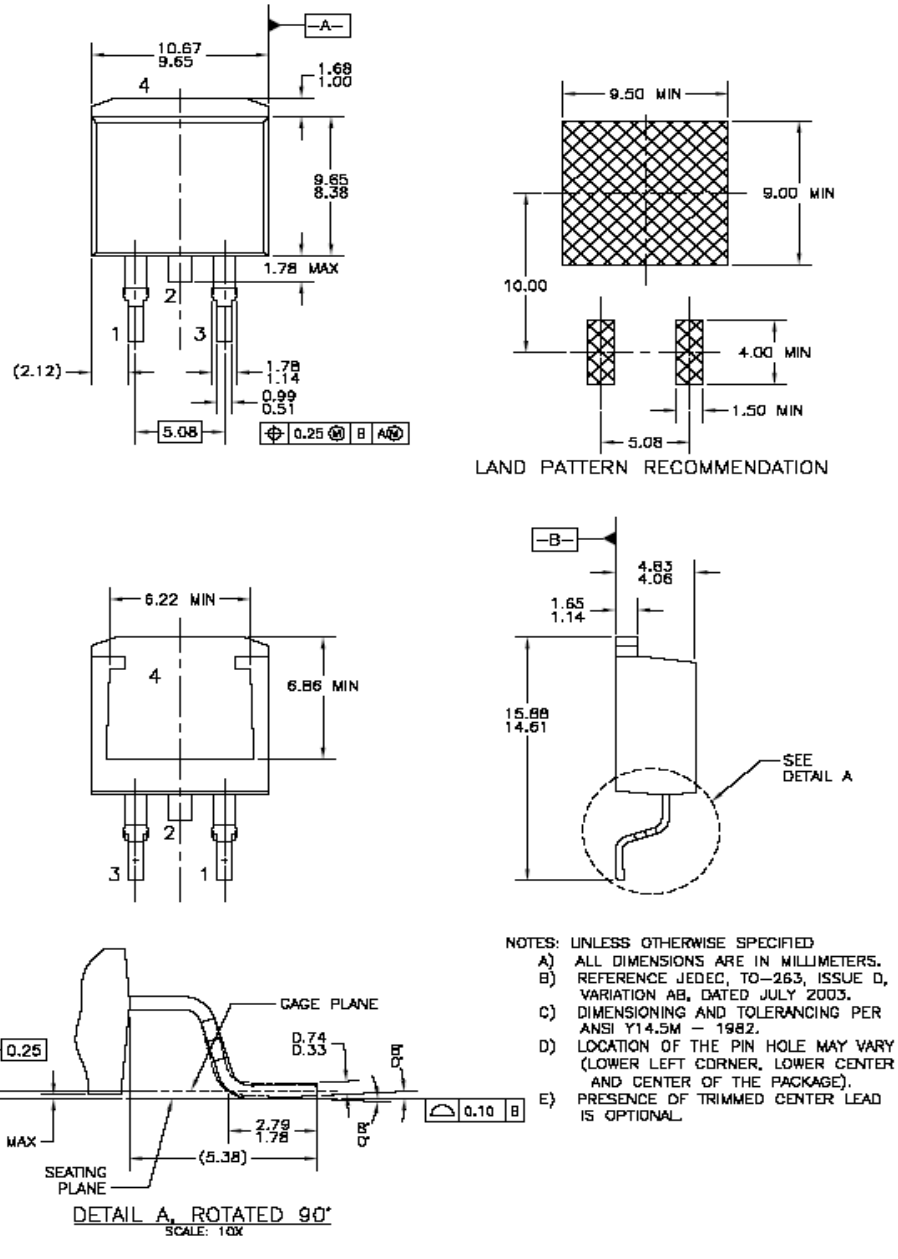
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Mechanical Dimensions

D2-PAK



NOTES: UNLESS OTHERWISE SPECIFIED
A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) REFERENCE JEDEC, TO-263, ISSUE D, VARIATION AB, DATED JULY 2003.
C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1982.
D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters

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