

# FDMA7672

## Single N-Channel PowerTrench® MOSFET

30 V, 9 A, 21 mΩ

### Features

- Max  $r_{DS(on)}$  = 21 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 9\text{ A}$
- Max  $r_{DS(on)}$  = 32 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 7\text{ A}$
- Low Profile - 0.8 mm maximum - in the new package MicroFET 2x2 mm
- Free from halogenated compounds and antimony oxides
- RoHS compliant

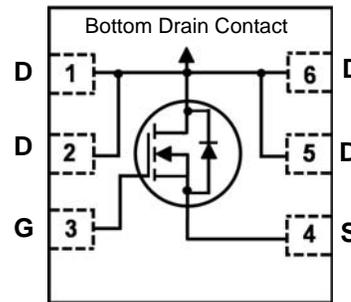
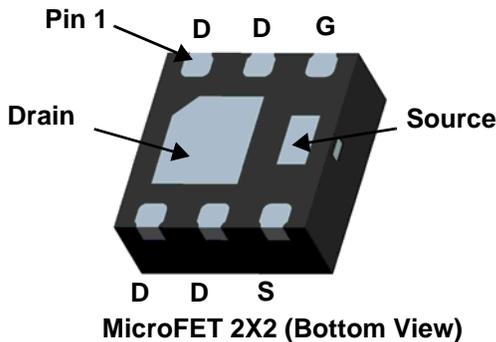


### General Description

This device has been designed to provide maximum efficiency and thermal performance for synchronous buck converters. The low  $r_{DS(on)}$  and gate charge provide excellent switching performance.

### Application

- DC – DC Buck Converters



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	30	V
$V_{GSS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous $T_A = 25\text{ °C}$ (Note 1a)	9	A
	-Pulsed	24	
$P_D$	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	2.4	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1b)	0.9	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
672	FDMA7672	MicroFET 2x2	7"	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		16		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	2.1	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 9\text{ A}$		14	21	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 7\text{ A}$		20	32	
		$V_{GS} = 10\text{ V}$ , $I_D = 9\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		19	28	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 9\text{ A}$		35		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ $f = 1.0\text{ MHz}$		570	760	pF
$C_{oss}$	Output Capacitance			195	260	pF
$C_{rss}$	Reverse Transfer Capacitance			25	40	pF
$R_g$	Gate Resistance			1.5		$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 9\text{ A}$ $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		6	12	ns
$t_r$	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			14	25	ns
$t_f$	Fall Time			2	10	ns
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$	$V_{DD} = 15\text{ V}$ , $I_D = 9\text{ A}$	9.3	13
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$	4.4		6	nC
$Q_{gs}$	Gate to Source Gate Charge		1.9			nC
$Q_{gd}$	Gate to Drain "Miller" Charge		1.5			nC

**Drain-Source Diode Characteristics**

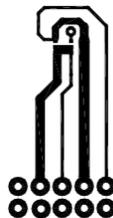
$I_S$	Maximum Continuous Drain-Source Diode Forward Current			2	A	
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2\text{ A}$ (Note 2)		0.8	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 9\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		18	32	ns
$Q_{rr}$	Reverse Recovery Charge			5	10	nC

## NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



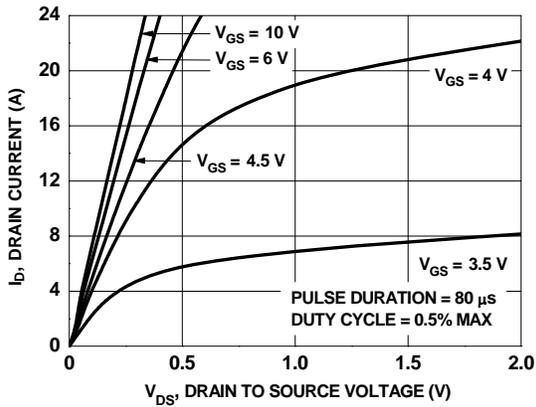
a.  $52\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.



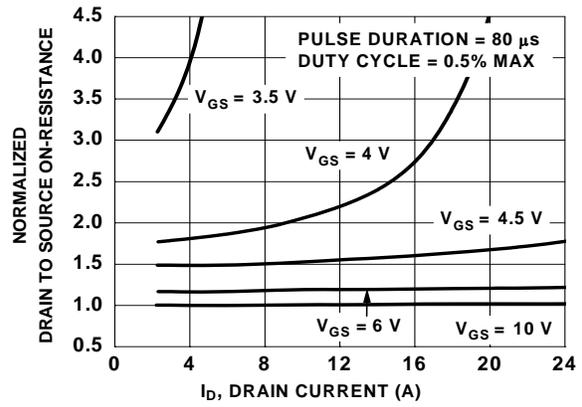
b.  $145\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.

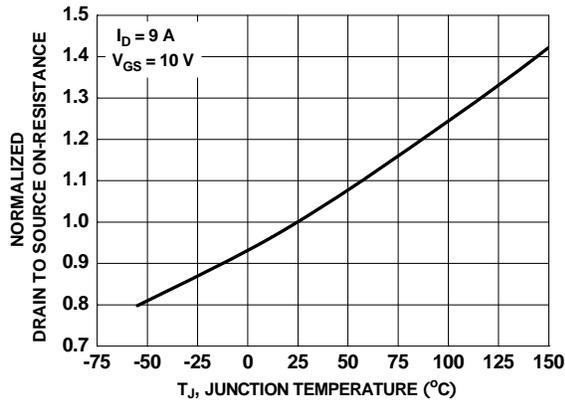
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



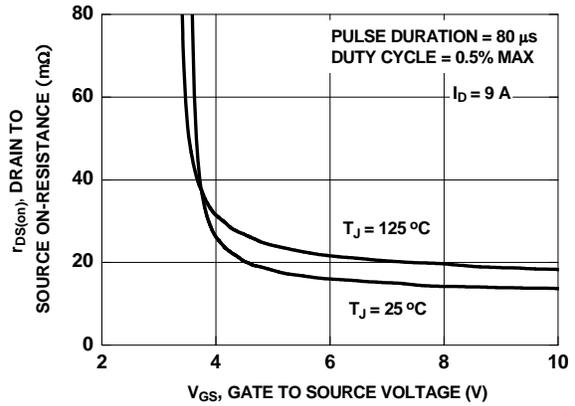
**Figure 1. On-Region Characteristics**



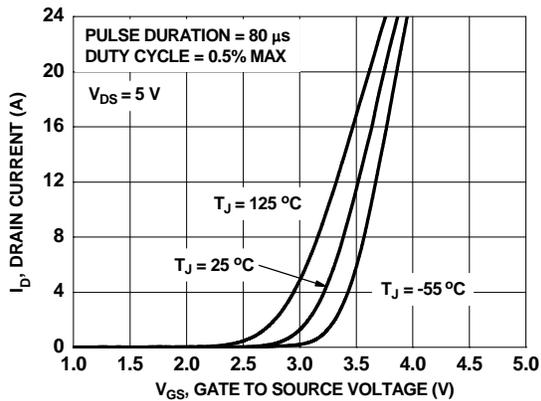
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



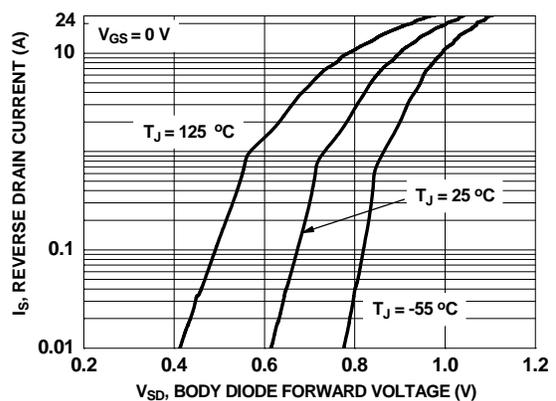
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

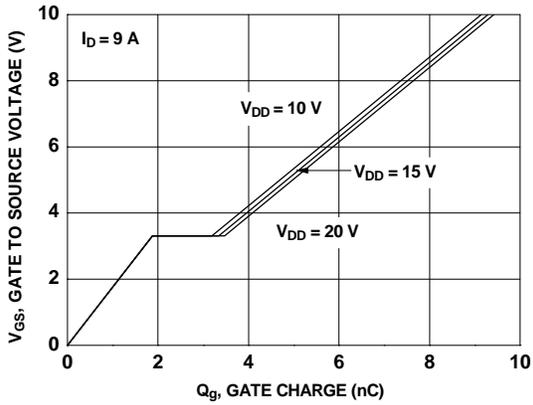


**Figure 5. Transfer Characteristics**

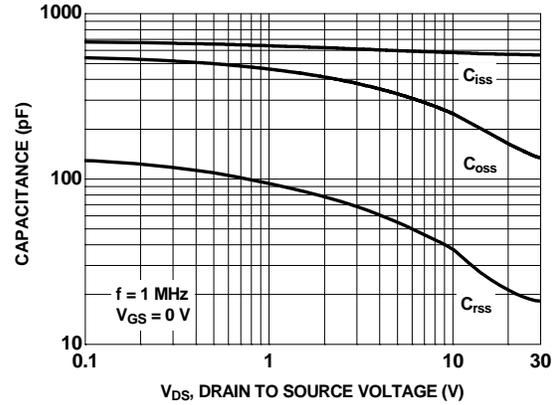


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

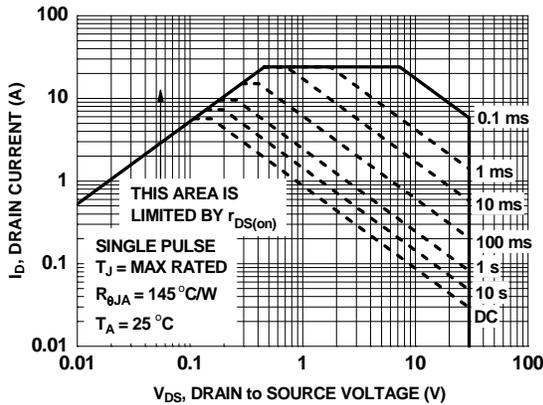
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



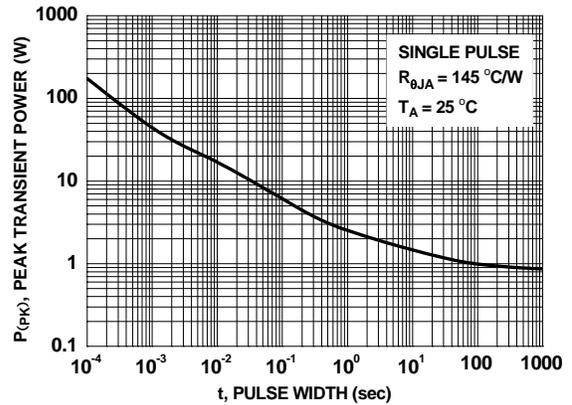
**Figure 7. Gate Charge Characteristics**



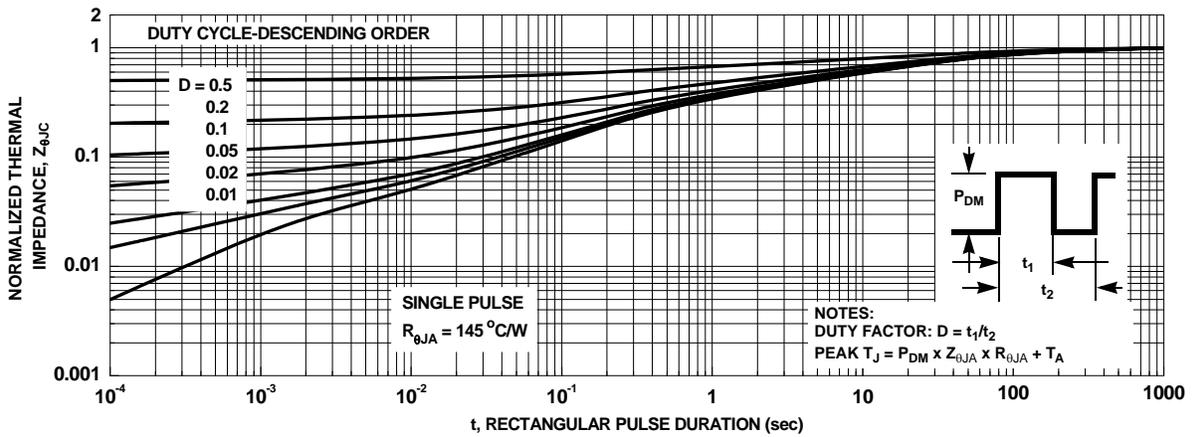
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Forward Bias Safe Operating Area**

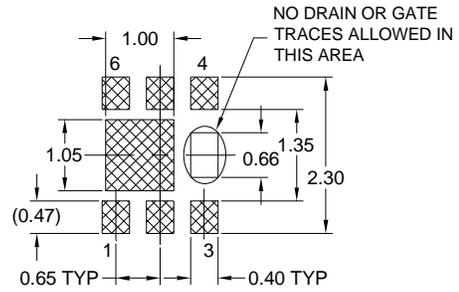
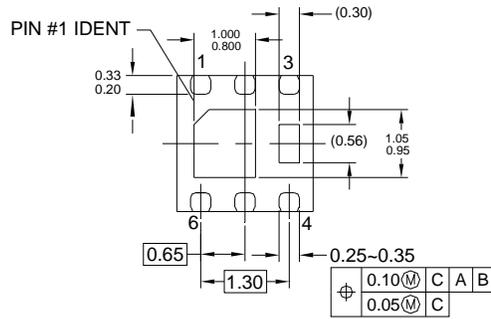
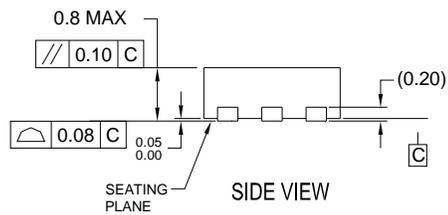
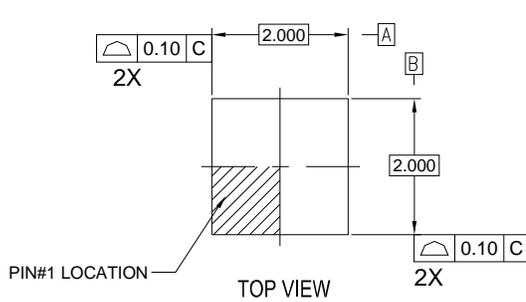


**Figure 10. Single Pulse Maximum Power Dissipation**

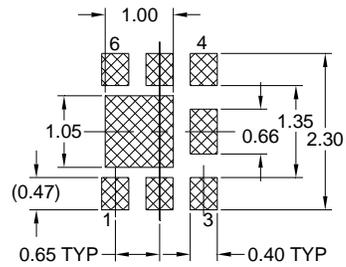


**Figure 11. Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout



RECOMMENDED LAND PATTERN OPT 1



RECOMMENDED LAND PATTERN OPT 2

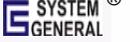
### NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-229 DATED AUG/2003
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994



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