

# FDMS86252

## N-Channel PowerTrench® MOSFET

### 150 V, 16 A, 51 mΩ

#### Features

- Max  $r_{DS(on)}$  = 51 mΩ at  $V_{GS} = 10$  V,  $I_D = 4.6$  A
- Max  $r_{DS(on)}$  = 70 mΩ at  $V_{GS} = 6$  V,  $I_D = 3.9$  A
- Advanced package and silicon combination for low  $r_{DS(on)}$  and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

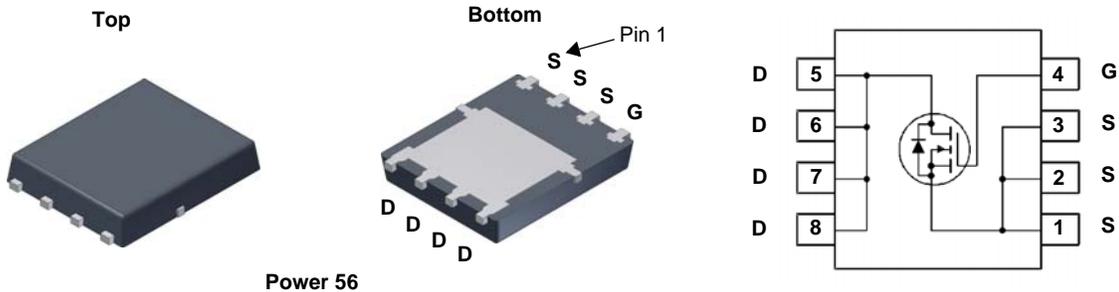


#### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

#### Application

- DC-DC Conversion



#### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Conditions	Rating	Units
$V_{DS}$	Drain to Source Voltage		150	V
$V_{GS}$	Gate to Source Voltage		±20	V
$I_D$	Drain Current -Continuous (Package limited)	$T_C = 25$ °C	16	A
	-Continuous (Silicon limited)	$T_C = 25$ °C	24	
	-Continuous	$T_A = 25$ °C (Note 1a)	4.6	
	-Pulsed		20	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	50	mJ
$P_D$	Power Dissipation	$T_C = 25$ °C	69	W
	Power Dissipation	$T_A = 25$ °C (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range		-55 to +150	°C

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86252	FDMS86252	Power 56	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		106		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	2.0	2.8	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-9		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4.6\text{ A}$		43.9	51	m $\Omega$
		$V_{GS} = 6\text{ V}$ , $I_D = 3.9\text{ A}$		50.5	70	
		$V_{GS} = 10\text{ V}$ , $I_D = 4.6\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		83	96	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 4.6\text{ A}$		15		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 75\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		678	905	pF
$C_{oss}$	Output Capacitance			74	115	pF
$C_{rss}$	Reverse Transfer Capacitance			4.3	10	pF
$R_g$	Gate Resistance			0.4		$\Omega$

### Switching Characteristics

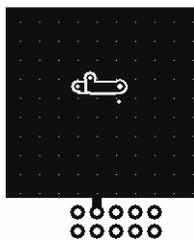
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\text{ V}$ , $I_D = 4.6\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		7.7	16	ns	
$t_r$	Rise Time			2.3	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			15	27	ns	
$t_f$	Fall Time			3.2	10	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		11	15	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 5\text{ V}$	$V_{DD} = 75\text{ V}$ , $I_D = 4.6\text{ A}$		6.1	8.6	nC
$Q_{gs}$	Gate to Source Charge				2.8		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				2.4		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2\text{ A}$ (Note 2)		0.75	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 4.6\text{ A}$ (Note 2)		0.80	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 4.6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		56	90	ns
$Q_{rr}$	Reverse Recovery Charge			61	98	nC

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $50\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.



b.  $125\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.

3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 10\text{ A}$ ,  $V_{DD} = 135\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

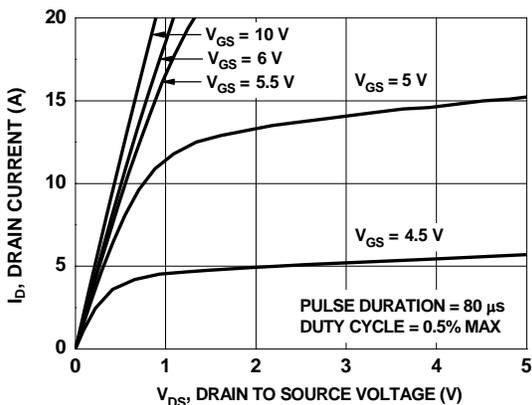


Figure 1. On Region Characteristics

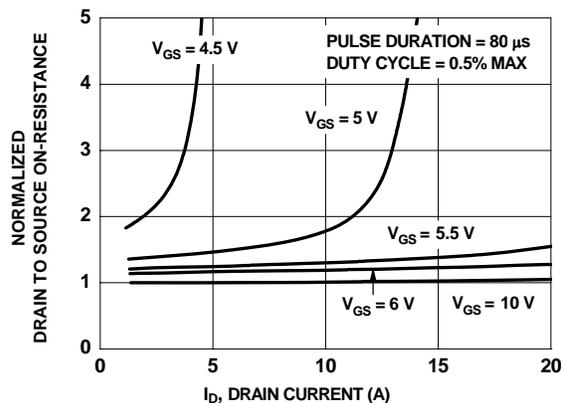


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

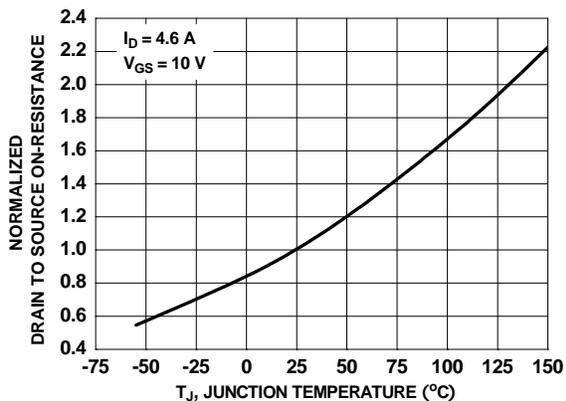


Figure 3. Normalized On Resistance vs Junction Temperature

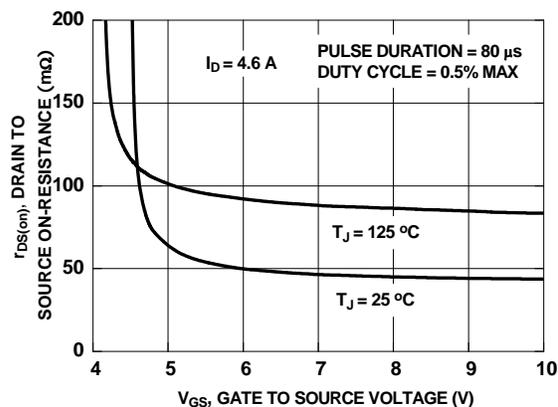


Figure 4. On-Resistance vs Gate to Source Voltage

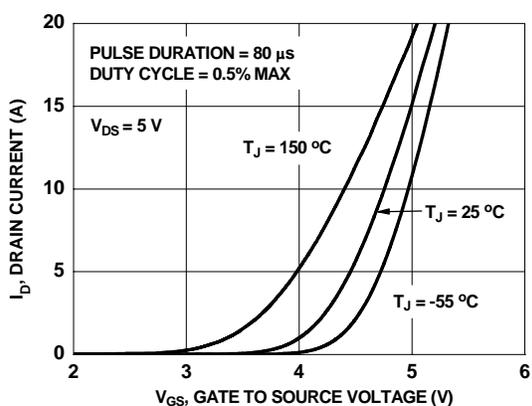


Figure 5. Transfer Characteristics

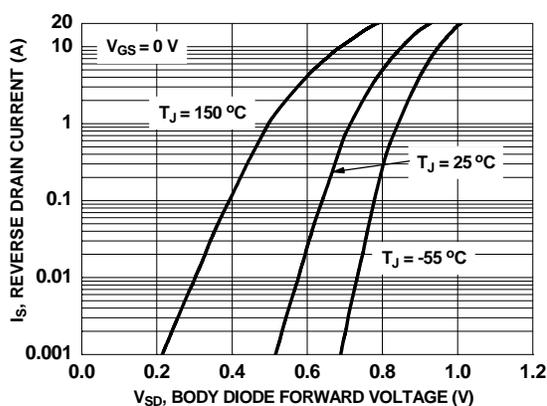
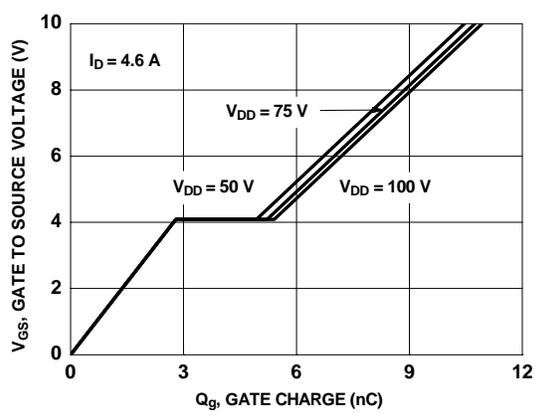
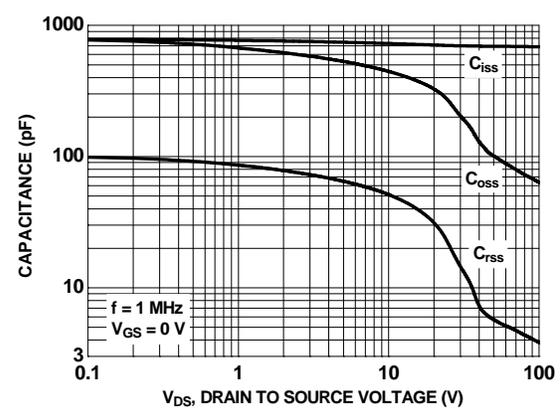


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

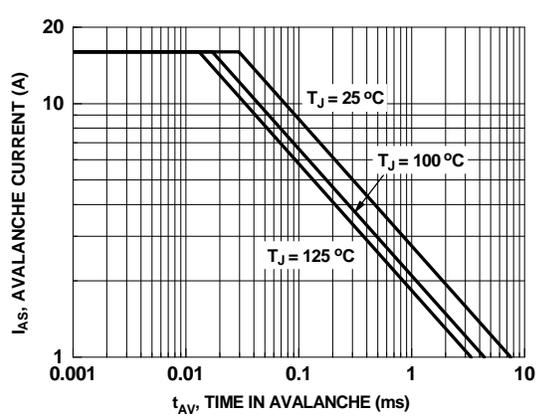
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



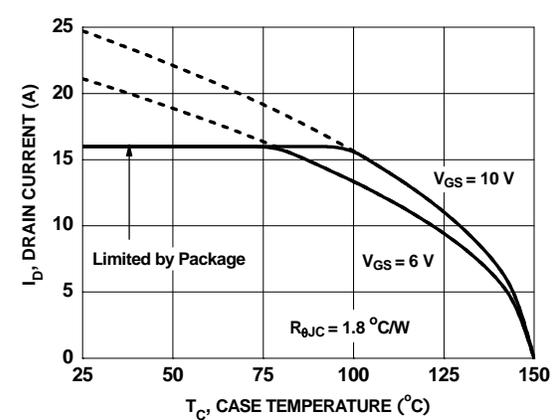
**Figure 7. Gate Charge Characteristics**



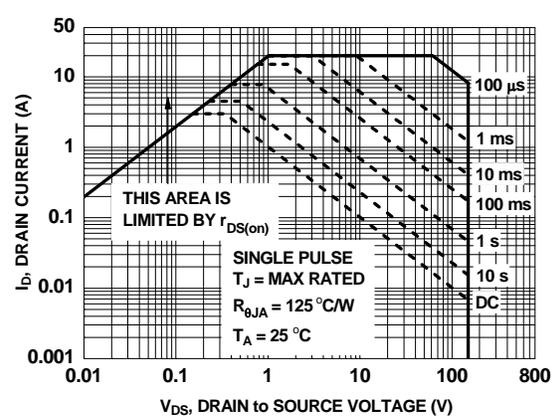
**Figure 8. Capacitance vs Drain to Source Voltage**



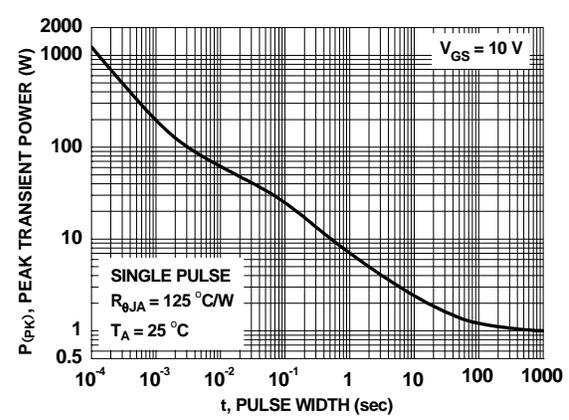
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

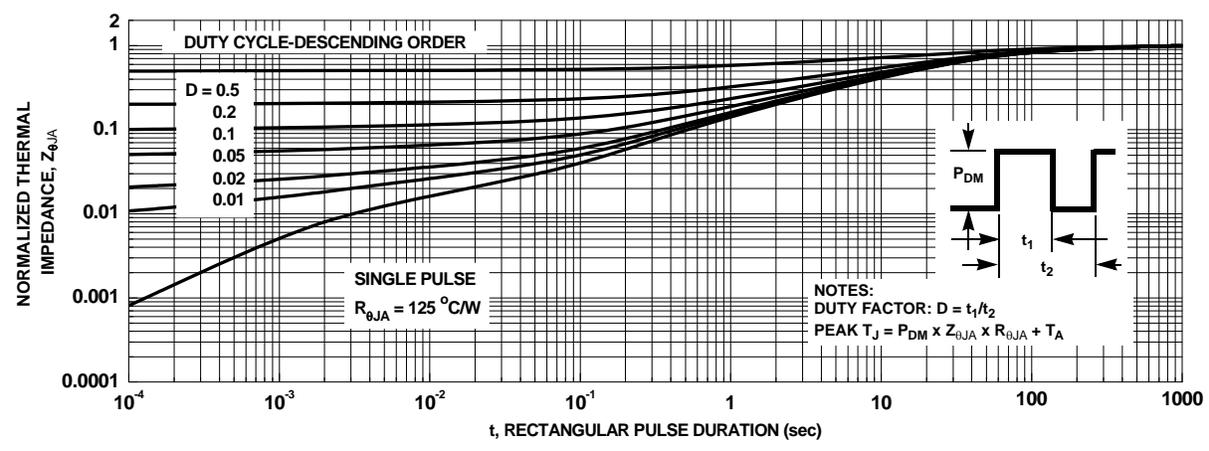


**Figure 11. Forward Bias Safe Operating Area**



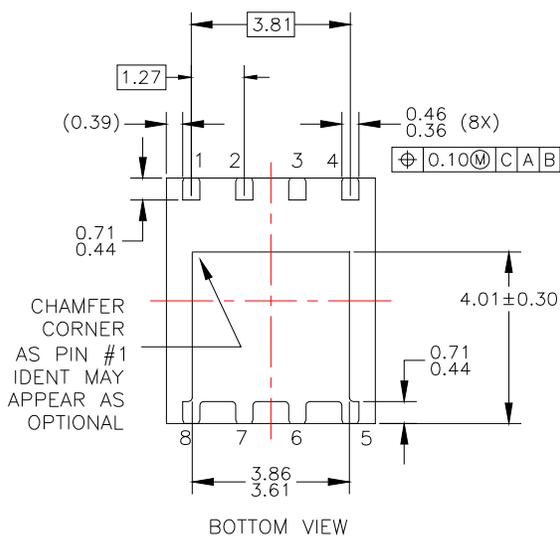
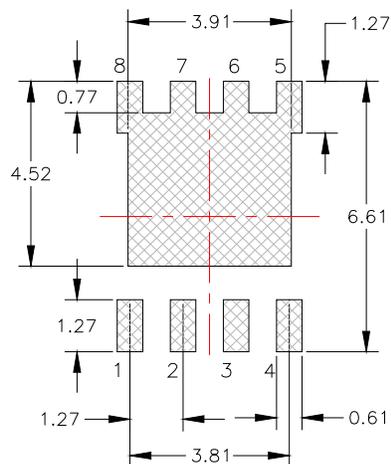
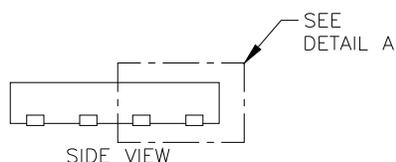
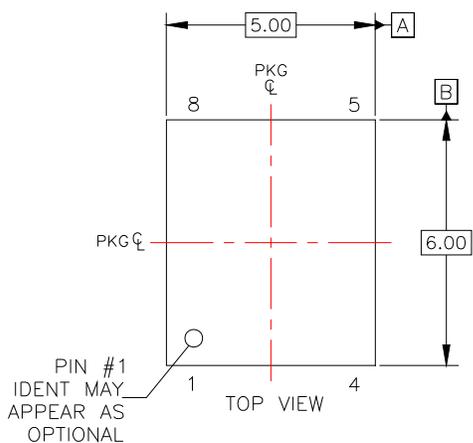
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

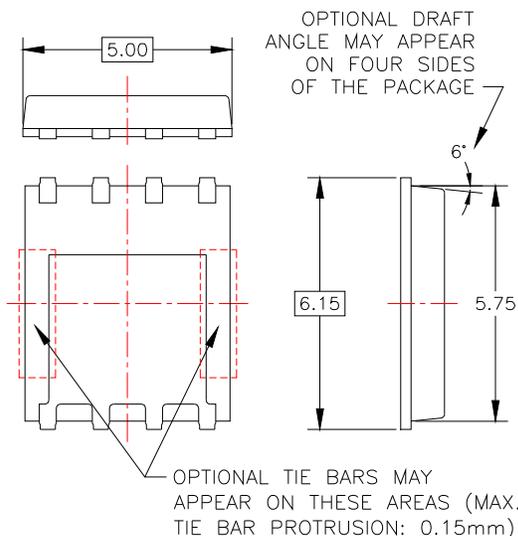


**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout

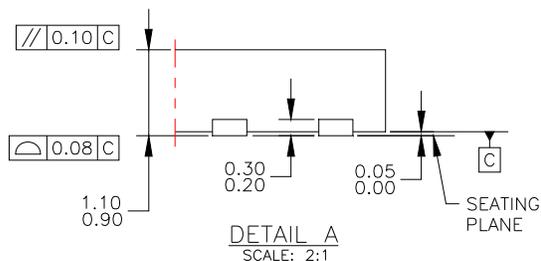


CHAMFER CORNER AS PIN #1 IDENT MAY APPEAR AS OPTIONAL



NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08AREV4





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Datasheet Identification	Product Status	Definition
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