

October 2012

FDMS8820

N-Channel PowerTrench[®] MOSFET 30 V, 116 A, 2.0 m Ω

Features

- Max $r_{DS(on)} = 2.0 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 28 \text{ A}$
- Max $r_{DS(on)} = 2.4 \text{ m}\Omega$ at $V_{GS} = 4.5 \text{ V}$, $I_D = 25 \text{ A}$
- \blacksquare Advanced Package and Silicon combination for low $r_{\text{DS}(\text{on})}$ and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

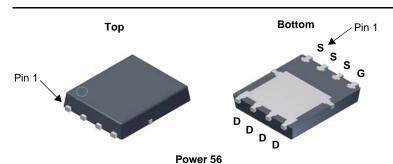


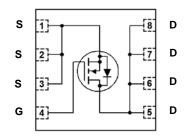
General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Applications

- VRM Vcore Switching for Desktop and Server
- OringFET / Load Switching
- DC-DC Conversion





MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V _{DS}	Drain to Source Voltage			30	V
V _{GS}	Gate to Source Voltage		(Note 4)	±20	V
	Drain Current -Continuous	T _C = 25 °C		116	
I _D	-Continuous	T _A = 25 °C	(Note 1a)	28	Α
	-Pulsed		(Note 5)	180	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	294	mJ
D	Power Dissipation	T _C = 25 °C		78	W
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	2.5	VV
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8820	FDMS8820	Power 56	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C		19		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1.2	1.5	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		-6		mV/°C
		V _{GS} = 10 V, I _D = 28 A		1.4	2.0	
r _{DS(on)} Static Drain to Source On Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 25 \text{ A}$		1.8	2.4	mΩ	
		V _{GS} = 10 V, I _D = 28 A, T _J = 125 °C		2.0	2.8	
9 _{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 28 \text{ A}$		76		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 45 V V 0 V		3995	5315	pF
C _{oss}	Output Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		1295	1725	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 101112		177	270	pF
R _q	Gate Resistance		0.1	1.1	2.5	Ω

Switching Characteristics

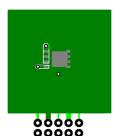
t _{d(on)}	Turn-On Delay Time		14	25	ns
t _r	Rise Time	V _{DD} = 15 V, I _D = 28 A,	7.7	16	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	41	66	ns
t _f	Fall Time		6.4	13	ns
Q_g	Total Gate Charge	V _{GS} = 0 V to 10 V	63	88	nC
Qg	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$ $V_{DD} = 15 \text{ V},$	30	42	nC
Q _{gs}	Gate to Source Charge	I _D = 28 A	9.8		nC
Q_{gd}	Gate to Drain "Miller" Charge		8.2		nC

Drain-Source Diode Characteristics

V _{SD} Source to Drain Diode Forward Vol	Source to Drain Diede Ferward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.0 \text{ A}$ (Note 2)		0.7	1.1	V
	Source to Drain blode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 28 \text{ A}$ (Note 2)		0.8	1.2	V
t _{rr}	Reverse Recovery Time	-I _F = 28 A, di/dt = 100 A/μs		43	69	ns
Q _{rr}	Reverse Recovery Charge	1F = 20 A, αι/αι = 100 A/μS		27	43	nC

Notes:

^{1.} $R_{\theta,IA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta,IC}$ is guaranteed by design while $R_{\theta,CA}$ is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

^{2.} Pulse Test: Pulse Width < 300 $\mu s,$ Duty cycle < 2.0%.

^{3.} E_{AS} of 294 mJ is based on starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 14 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 45 A.

^{4.} As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

^{5.} Pulsed Id limited by junction temperature,td<=100uS, please refer to SOA curve for more details.

Typical Characteristics T_J = 25 °C unless otherwise noted

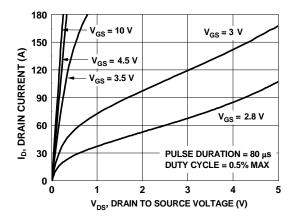


Figure 1. On Region Characteristics

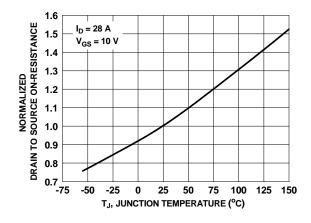


Figure 3. Normalized On Resistance vs Junction Temperature

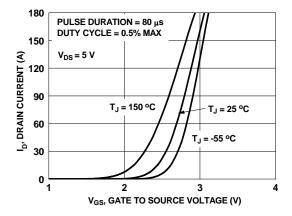


Figure 5. Transfer Characteristics

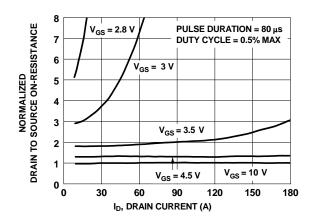


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

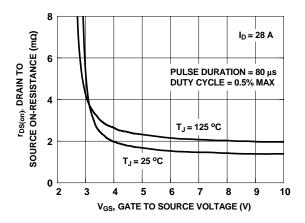


Figure 4. On-Resistance vs Gate to Source Voltage

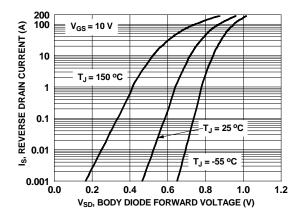


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

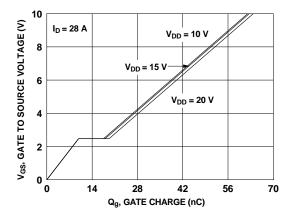


Figure 7. Gate Charge Characteristics

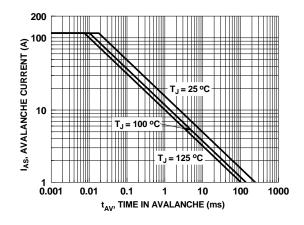


Figure 9. Unclamped Inductive Switching Capability

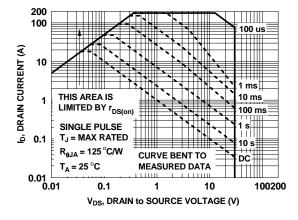


Figure 11. Forward Bias Safe Operating Area

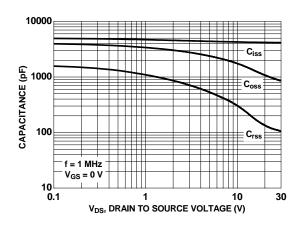


Figure 8. Capacitance vs Drain to Source Voltage

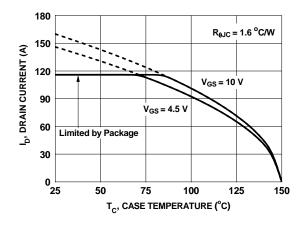


Figure 10. Maximum Continuous Drain Current vs Case Temperature

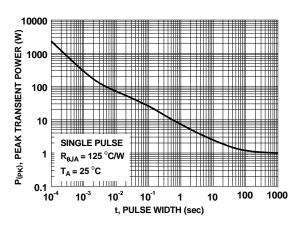


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25$ °C unless otherwise noted

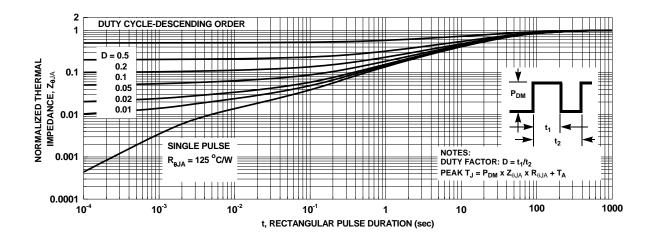
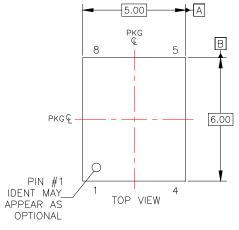
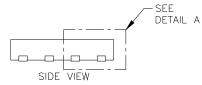
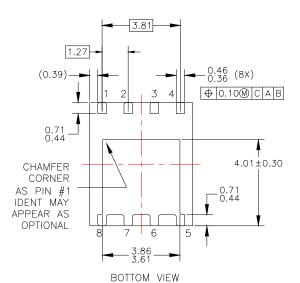


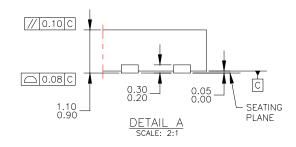
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

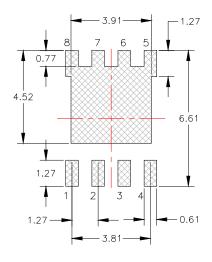
Dimensional Outline and Pad Layout



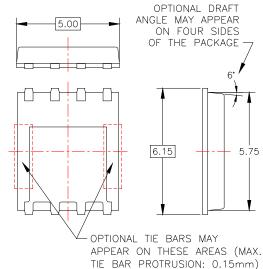








LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

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 DIMENSIONS DO NOT INCLUDE BURRS
 OR MOLD FLASH. MOLD FLASH OR
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- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
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