November 2012

FDP023N08B_F102

N-Channel PowerTrench® MOSFET

75V, 242A, 2.35mΩ

Features

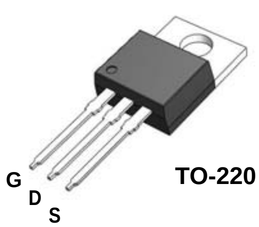
- $R_{DS(on)}$ = 1.96mΩ (Typ.) @ V_{GS} = 10V, I_D = 75A
- Low FOM $R_{DS(on)}$*Q_G
- Low reverse recovery charge, Q_{rr}
- Soft reverse recovery body diode
- Enables highly efficiency in synchronous rectification
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

Description

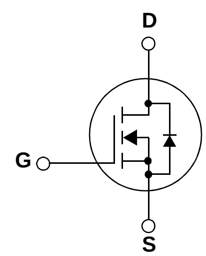
This N-Channel MOSFET is produced using Fairchild Semiconductor®'s advance PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Application

- Synchronous Rectification
- Battery Charger and Battery Protection circuit
- DC motor drives and Uninterruptible Power Supplies
- Micro Solar Inverter



TO-220



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter		FDP023N08B_F102	Units
V_{DSS}	Drain to Source Voltage		75	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	-Continuous (T_C = 25°C, Silicon Limited)	242*	A
		-Continuous (T_C = 100°C, Silicon Limited)	171*	
		-Continuous (T_C = 25°C, Package Limited)	120	
I_{DM}	Drain Current	- Pulsed (Note 1)	968	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		961	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6	V/ns
P_D	Power Dissipation	(T_C = 25°C)	245	W
		- Derate above 25°C	1.64	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

* Package limitation current is 120A.

Thermal Characteristics

Symbol	Parameter	FDP023N08B_F102	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.61	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Description	Quantity
FDP023N08B	FDP023N08B_F102	TO-220	F102: Trimmed Leads	50

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$, $T_C = 25^oC$	75	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25^oC	-	0.35	-	$V/^oC$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60V$, $V_{GS} = 0V$	-	-	1	μA
		$V_{DS} = 60V$, $T_C = 150^oC$	-	-	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	-	-	±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2.0	-	3.8	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 75A$	-	1.96	2.35	mΩ
g_{FS}	Forward Transconductance	$V_{DS} = 10V$, $I_D = 75A$	-	185	-	S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{iss}	Input Capacitance	$V_{DS} = 37.5V$, $V_{GS} = 0V$ f = 1MHz	-	10350	13765	pF
C_{oss}	Output Capacitance		-	1855	2465	pF
C_{rss}	Reverse Transfer Capacitance		-	46.8	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 37.5V$, $V_{GS} = 0V$	-	3290	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 37.5V$, $I_D = 100A$ $V_{GS} = 10V$ (Note 4)	-	150	195	nC
Q_{gs}	Gate to Source Gate Charge		-	50.3	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	31.7	-	nC
$V_{plateau}$	Gate Plateau Volatge		-	4.9	-	V
Q_{sync}	Total Gate Charge Sync.	$V_{DS} = 0V$, $I_D = 50A$ (Note 5)	-	127.4	-	nC
Q_{oss}	Output Charge	$V_{DS} = 37.5V$, $V_{GS} = 0V$	-	146.2	-	nC

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 37.5V$, $I_D = 100A$ $V_{GS} = 10V$, $R_{GEN} = 4.7\Omega$ (Note 4)	-	41	92	ns
t_r	Turn-On Rise Time		-	71	151	ns
$t_{d(off)}$	Turn-Off Delay Time		-	111	232	ns
t_f	Turn-Off Fall Time		-	56	122	ns
ESR	Equivalent Series Resistance (G-S)	f = 1MHz	-	2.23	-	Ω

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	242*	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	968	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 75A$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $V_{DD}=37.5V$, $I_{SD} = 100A$ $dI_F/dt = 100A/\mu s$	-	79.3	-	ns
Q_{rr}	Reverse Recovery Charge		-	114	-	nC

Notes:
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 3mH, $I_{AS} = 25.32A$, Starting $T_J = 25°C$
3. $I_{SD} \leq 100A$, $di/dt \leq 200A/\mu s$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$
4. Essentially Independent of Operating Temperature Typical Characteristics
5. See the test circuit in page 8

Typical Performance Characteristics

Figure 1. On-Region Characteristics

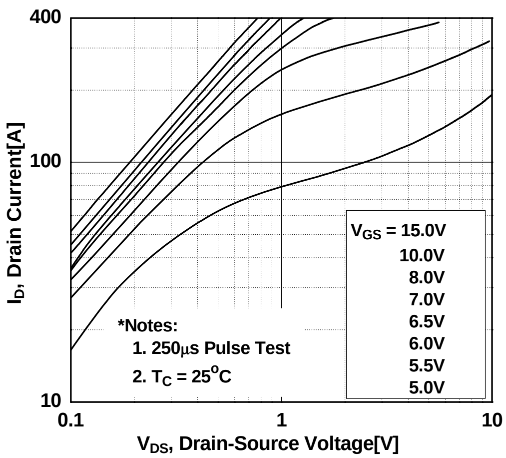


Figure 2. Transfer Characteristics

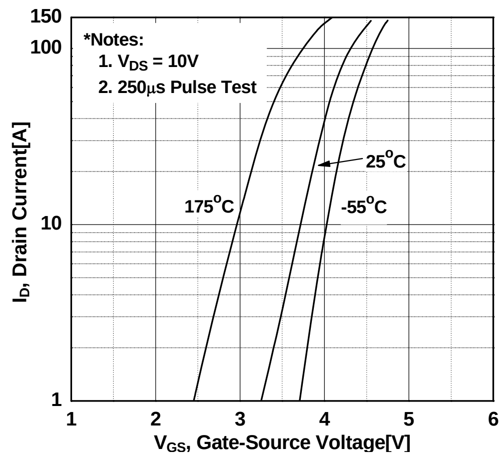


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

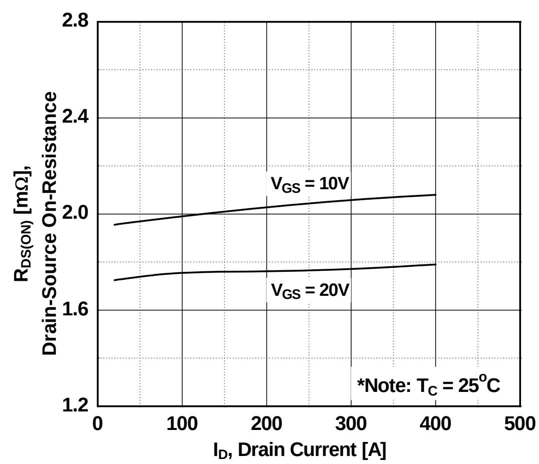


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

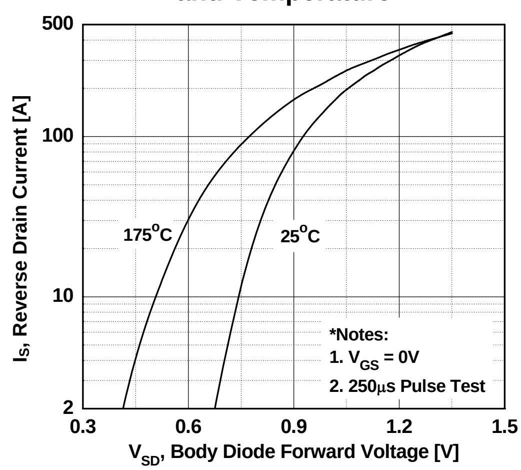


Figure 5. Capacitance Characteristics

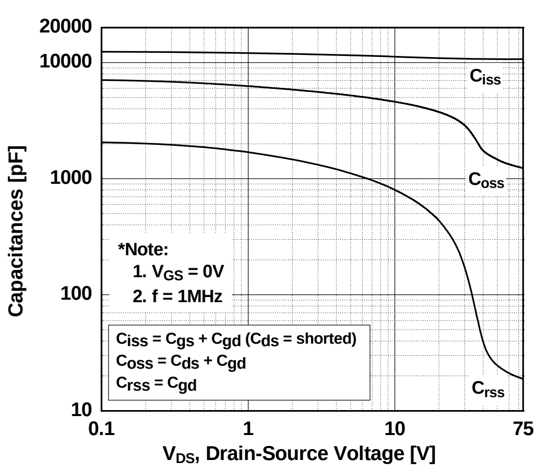
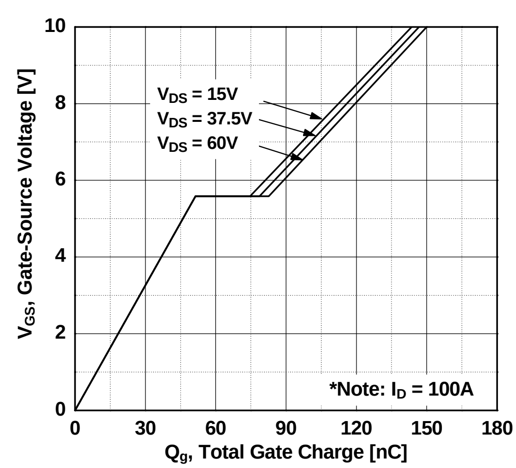


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

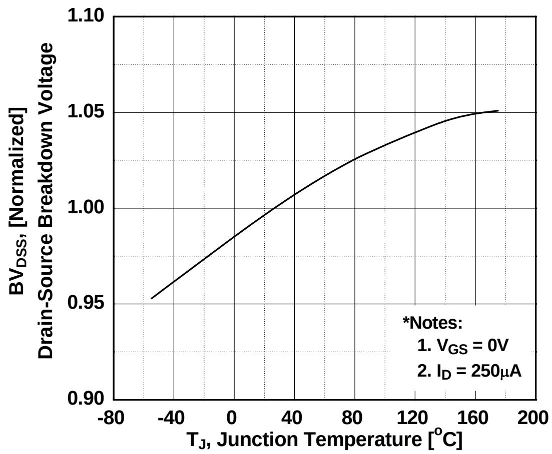


Figure 8. On-Resistance Variation vs. Temperature

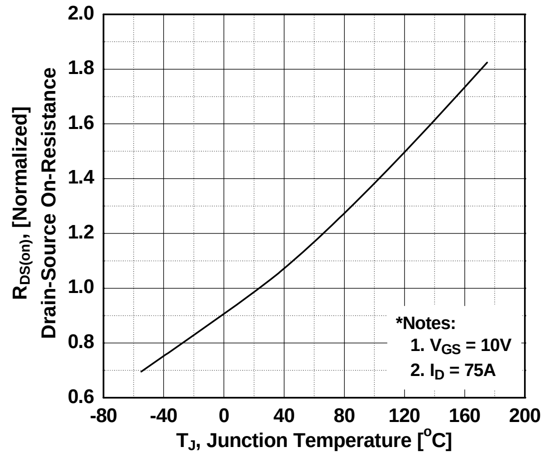


Figure 9. Maximum Safe Operating Area vs. Case Temperature

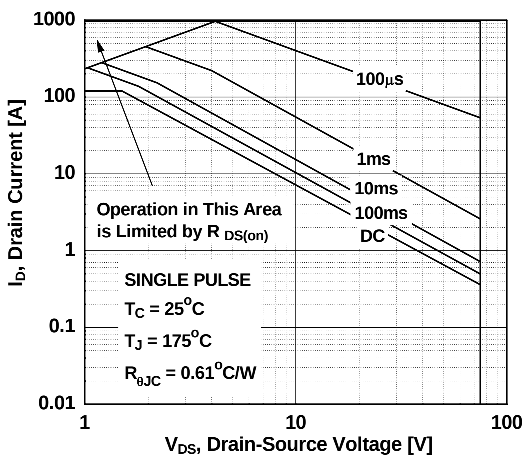


Figure 10. Maximum Drain Current

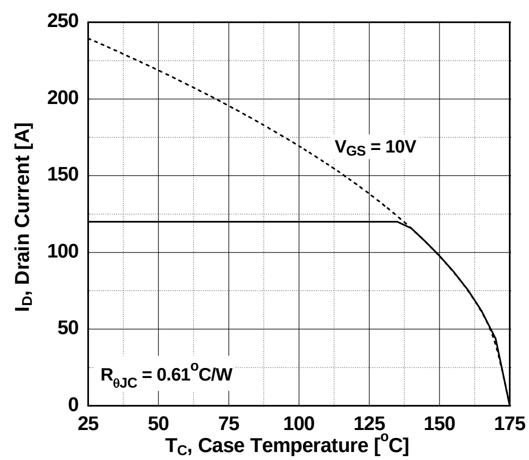


Figure 11. Eoss vs. Drain to Source Voltage

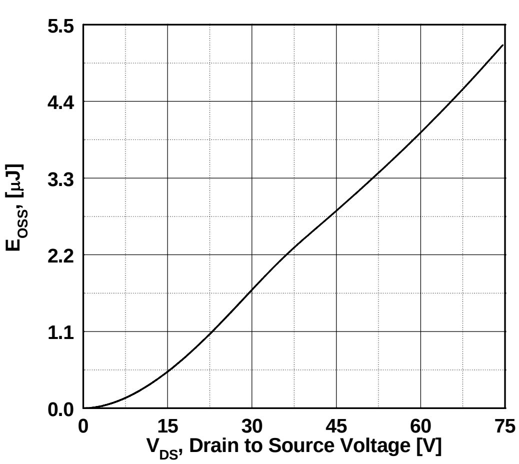
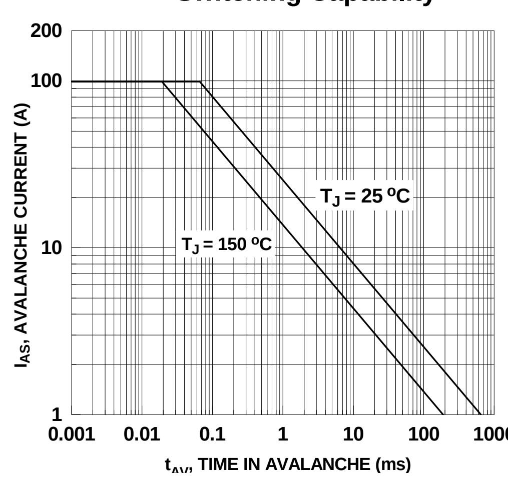
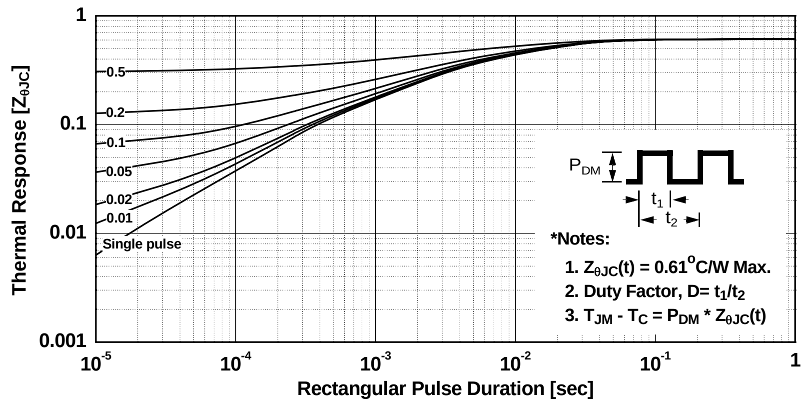


Figure 12. Unclamped Inductive Switching Capability

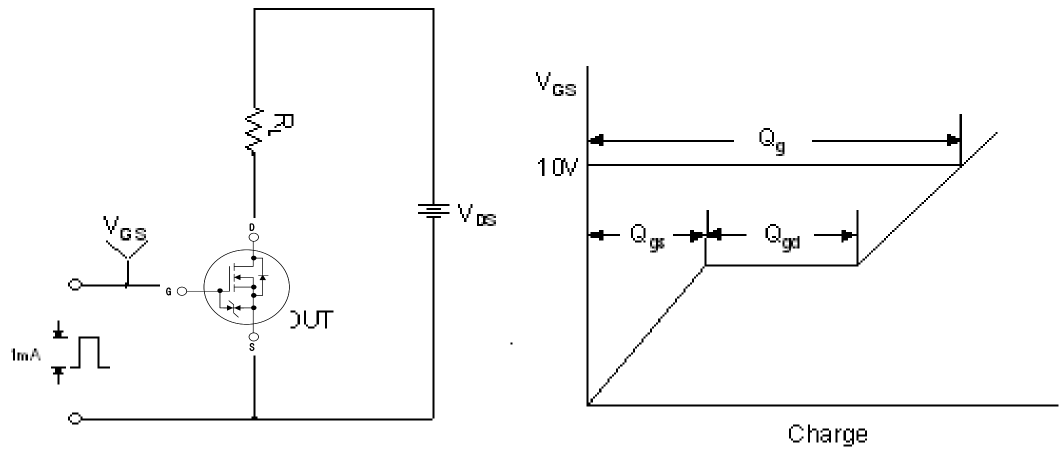


Typical Performance Characteristics (Continued)

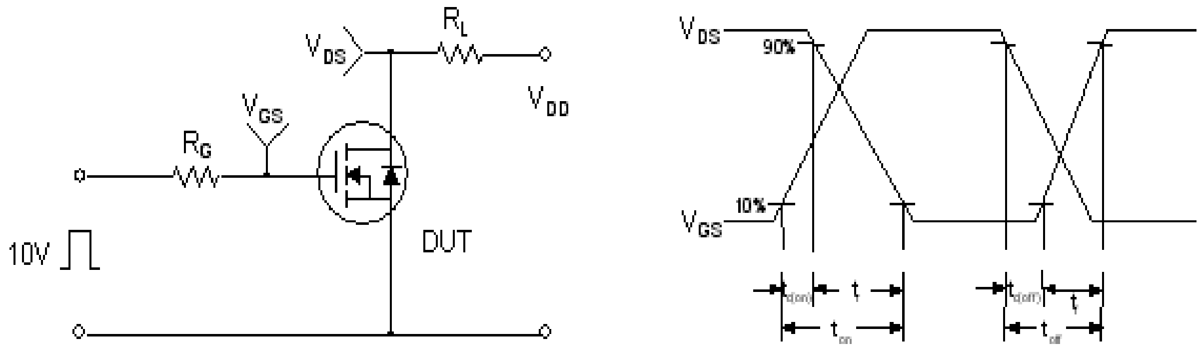
Figure 13. Transient Thermal Response Curve



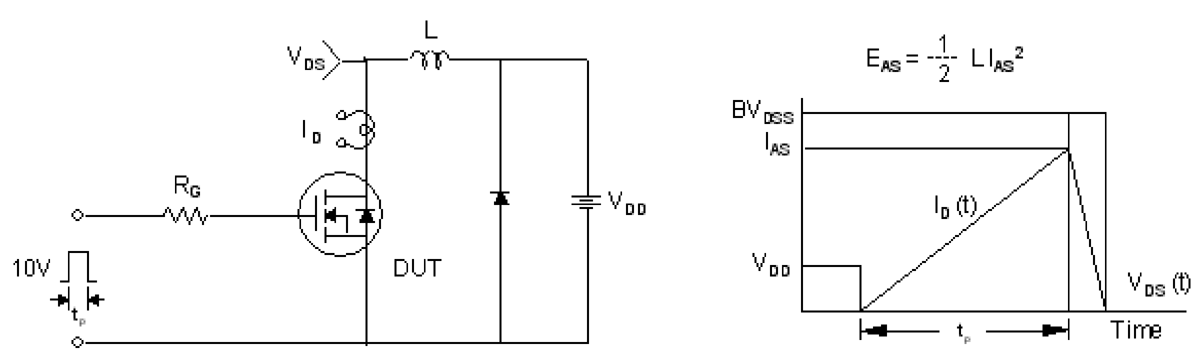
Gate Charge Test Circuit & Waveform



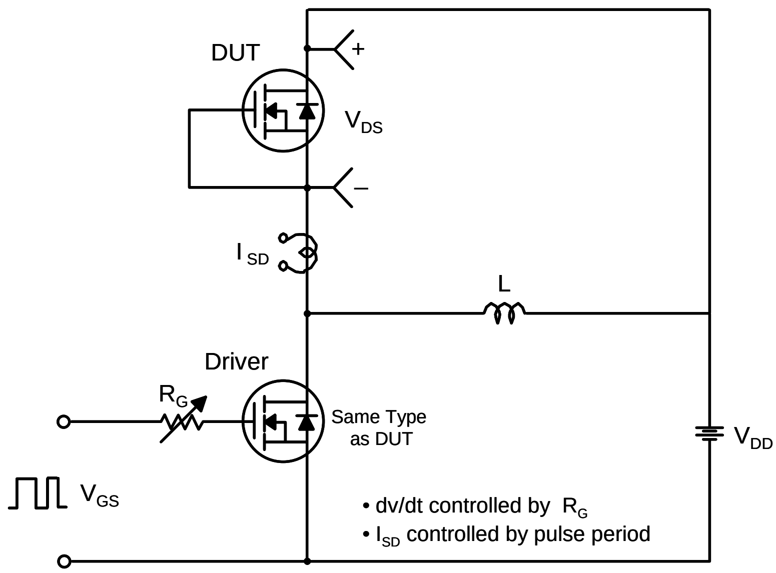
Resistive Switching Test Circuit & Waveforms

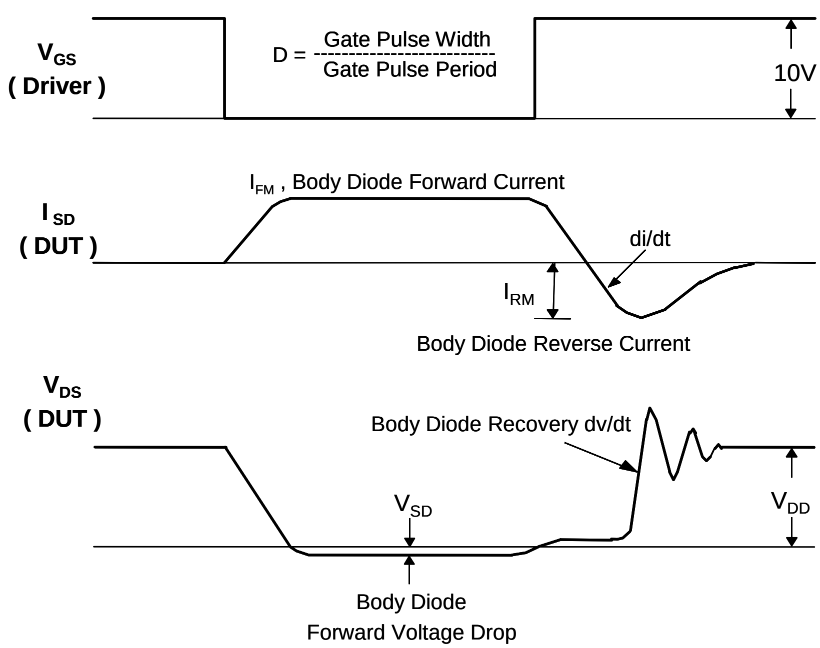


Unclamped Inductive Switching Test Circuit & Waveforms

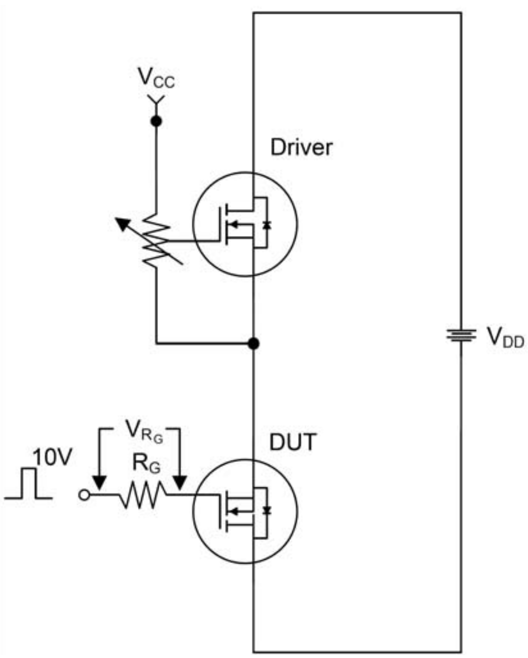


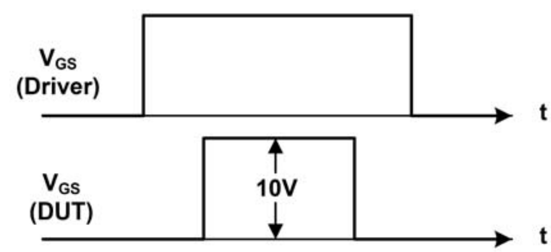
Peak Diode Recovery dv/dt Test Circuit & Waveforms





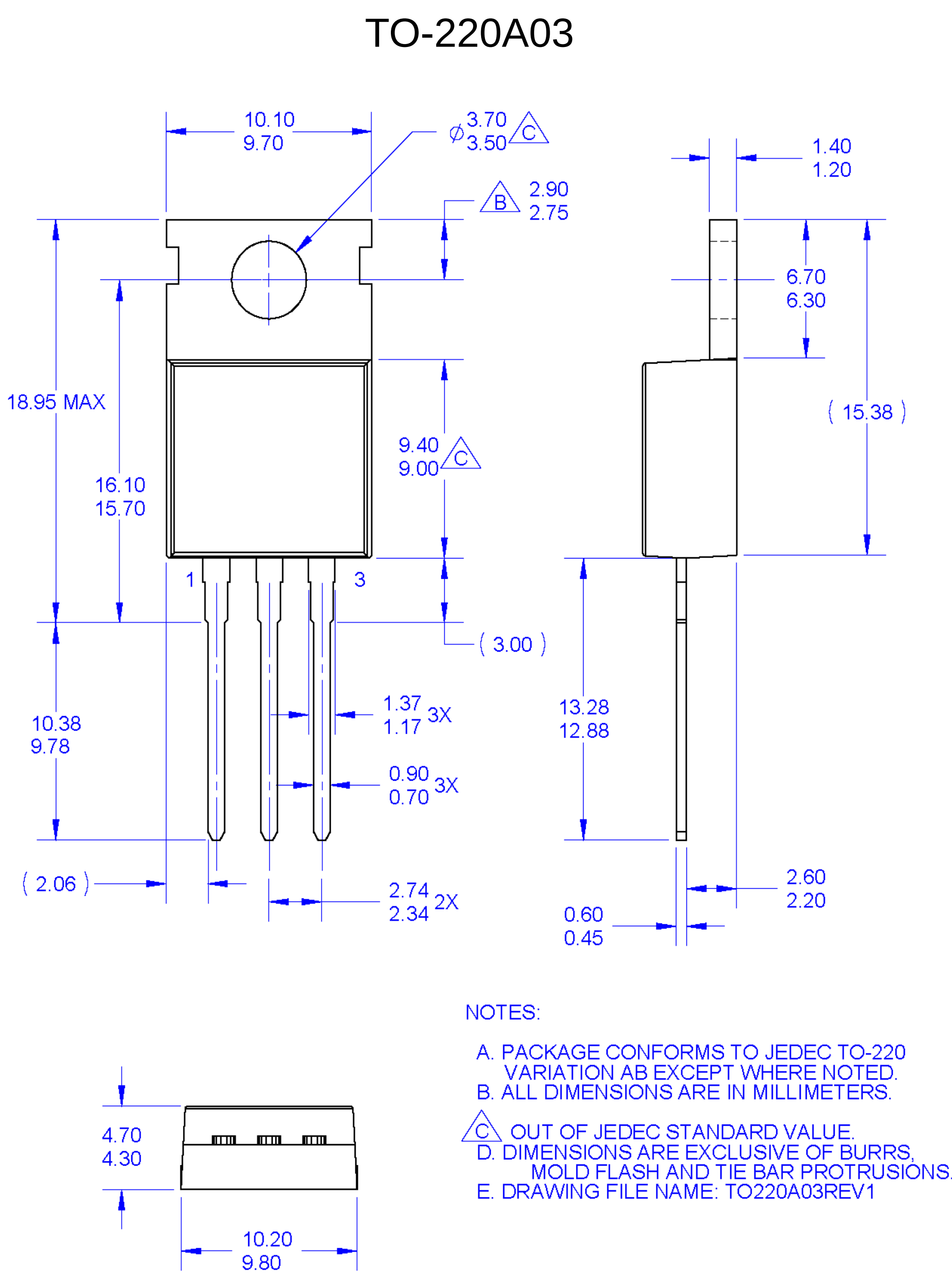
Total Gate Charge Qsync. Test Circuit & Waveforms





$$Qsync = \frac{1}{R_G} \cdot \int V_{R_G}(t)\ dt$$

Mechanical Dimensions



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C. OUT OF JEDEC STANDARD VALUE.
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I61