August 2012

FDP040N06

N-Channel PowerTrench® MOSFET

60V, 168A, 4.0mΩ

Features

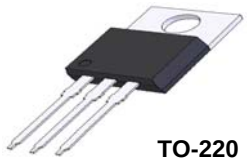
- $R_{DS(on)}$ = 3.2mΩ (Typ.) @ V_{GS} = 10V, I_D = 75A
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

General Description

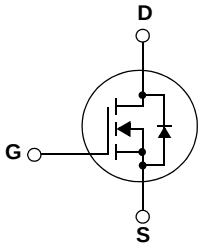
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

- DC to DC convertors / Synchronous Rectification



TO-220
FDP Series



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		FDP040N06	Units
V_{DSS}	Drain to Source Voltage		60	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	-Continuous (T_C = 25°C, Silicion Limited)	168*	A
		-Continuous (T_C = 100°C, Silicion Limited)	118*	
		-Continuous (T_C = 25°C, Package Limited)	120	
I_{DM}	Drain Current	- Pulsed (Note 1)	672	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	872	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	7.0	V/ns
P_D	Power Dissipation	(T_C = 25°C)	231	W
		- Derate above 25°C	1.54	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

Thermal Characteristics

Symbol	Parameter	FDP040N06	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.65	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP040N06	FDP040N06	TO-220	Tube	-	50

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$, $T_C = 25^oC$	60	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25^oC	-	0.04	-	$V/^oC$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60V$, $V_{GS} = 0V$	-	-	1	μA
		$V_{DS} = 60V$, $V_{GS} = 0V$, $T_C = 150^oC$	-	-	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 75A$	-	3.2	4.0	mΩ
g_{FS}	Forward Transconductance	$V_{DS} = 10V$, $I_D = 75A$	-	169	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz	-	6190	8235	pF
C_{oss}	Output Capacitance		-	900	1195	pF
C_{rss}	Reverse Transfer Capacitance		-	385	580	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 48V$, $I_D = 75A$, $V_{GS} = 10V$ (Note 4)	-	102	133	nC
Q_{gs}	Gate to Source Gate Charge		-	32	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	32	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30V$, $I_D = 75A$, $V_{GS} = 10V$, $R_{GEN} = 4.7\Omega$ (Note 4)	-	30	70	ns
t_r	Turn-On Rise Time		-	40	90	ns
$t_{d(off)}$	Turn-Off Delay Time		-	55	120	ns
t_f	Turn-Off Fall Time		-	24	58	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	168	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	672	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 75A$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 75A$, $dI_F/dt = 100A/\mu s$	-	41	-	ns
Q_{rr}	Reverse Recovery Charge		-	47	-	nC

Notes:
1: Repetitive Rating: Pulse width limited by maximum junction temperature
2: L = 0.31mH, $I_{AS} = 75A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25°C$
3: $I_{SD} \leq 75A$, $di/dt \leq 200A/\mu s$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$
4: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

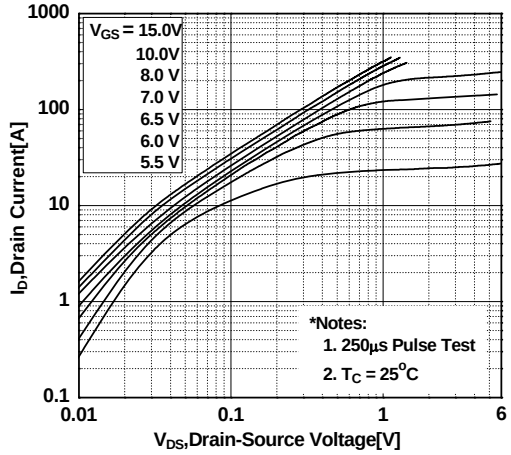


Figure 2. Transfer Characteristics

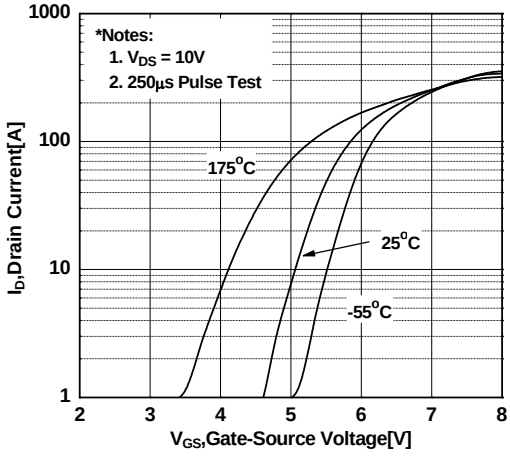


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

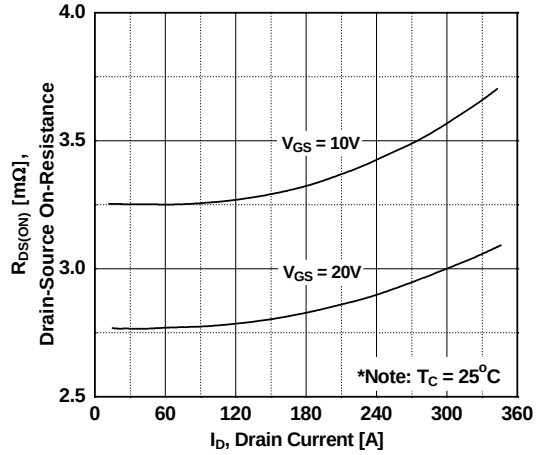


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

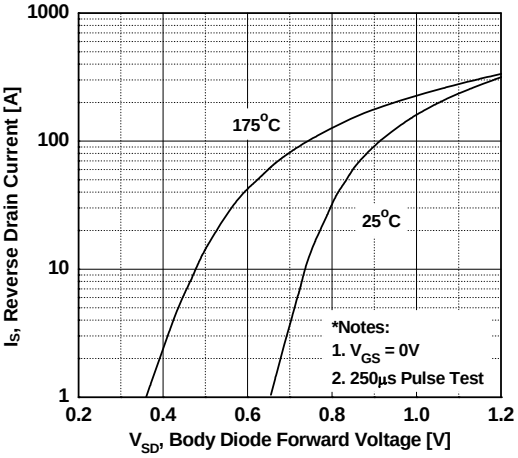


Figure 5. Capacitance Characteristics

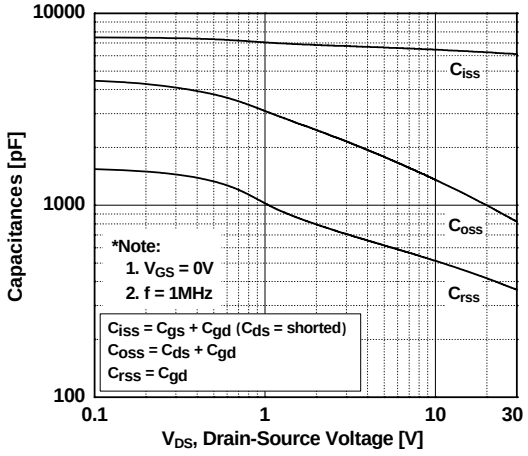
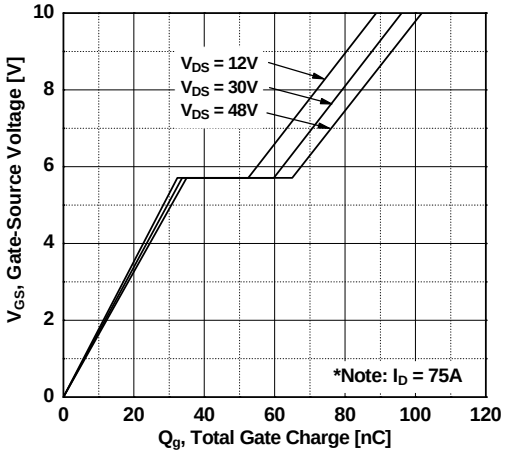


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

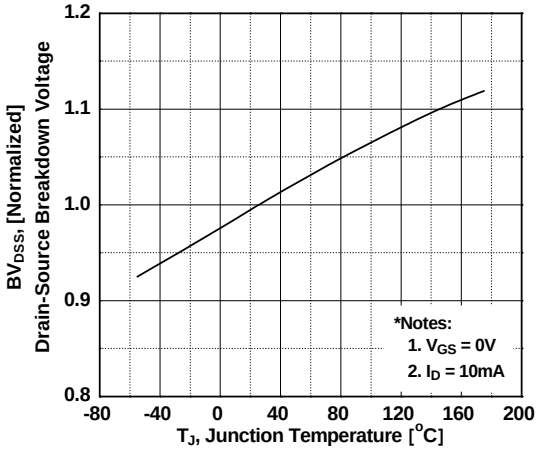


Figure 8. On-Resistance Variation vs. Temperature

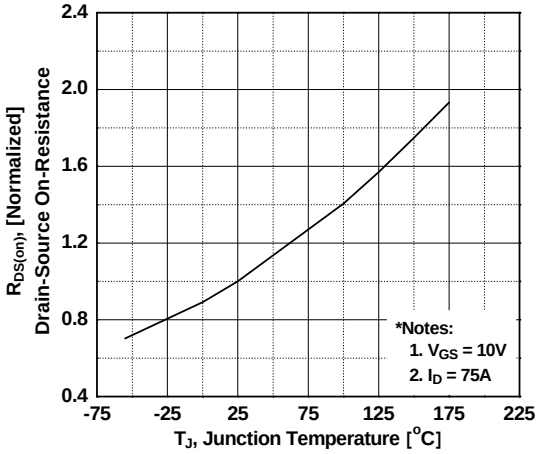


Figure 9. Maximum Safe Operating Area

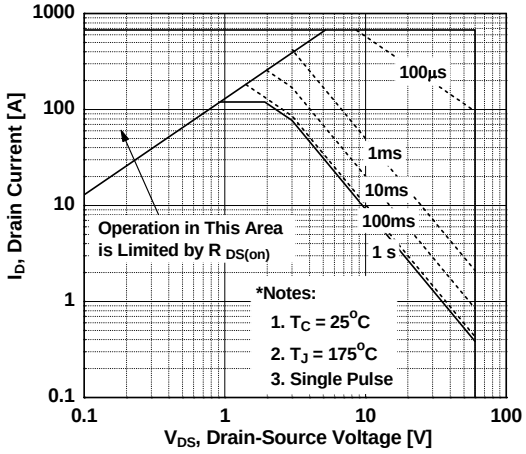


Figure 10. Maximum Drain Current vs. Case Temperature

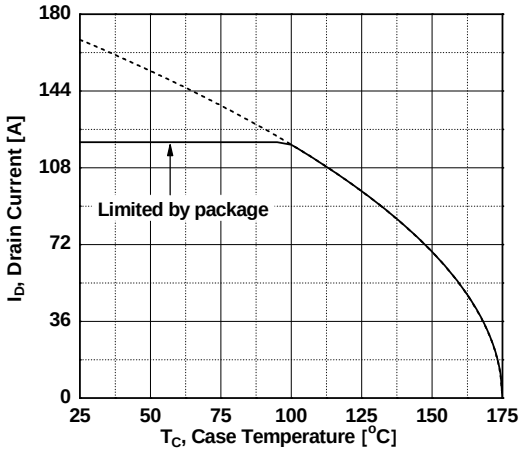
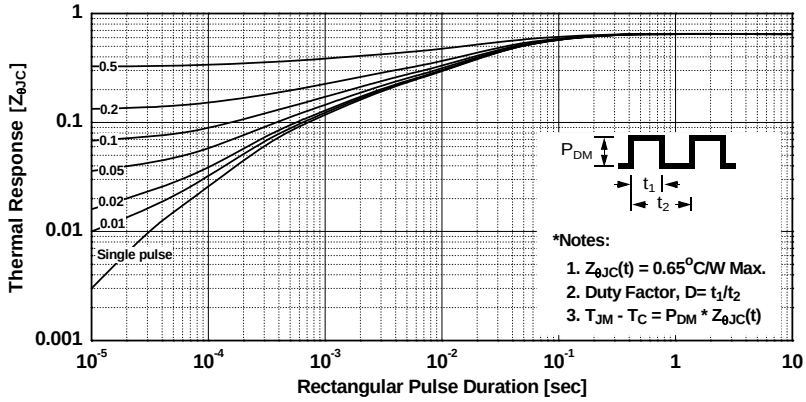
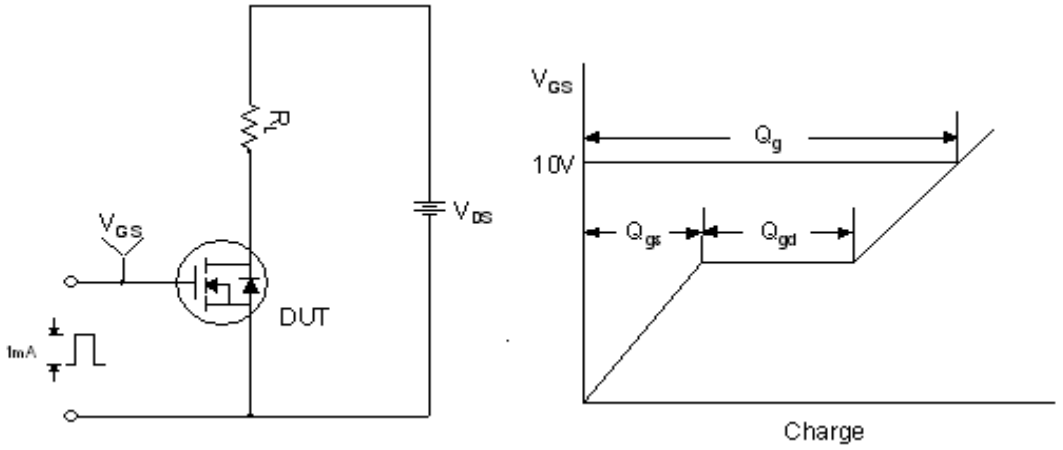


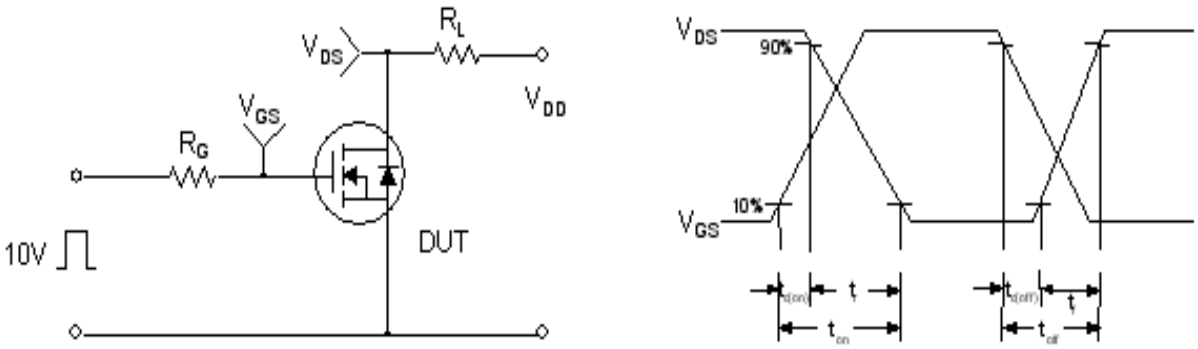
Figure 11. Transient Thermal Response Curve



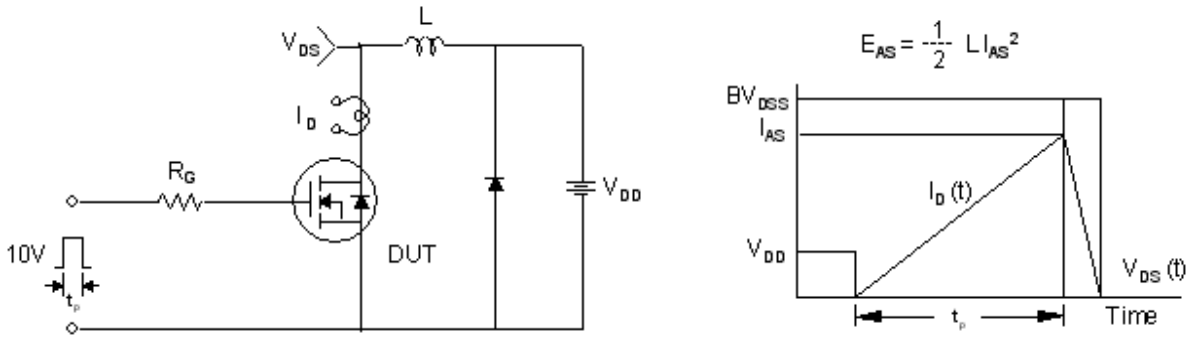
Gate Charge Test Circuit & Waveform



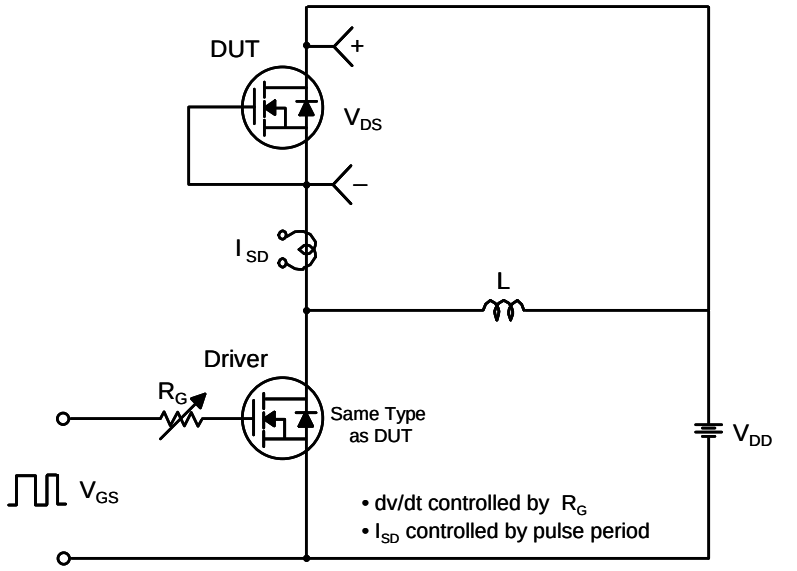
Resistive Switching Test Circuit & Waveforms

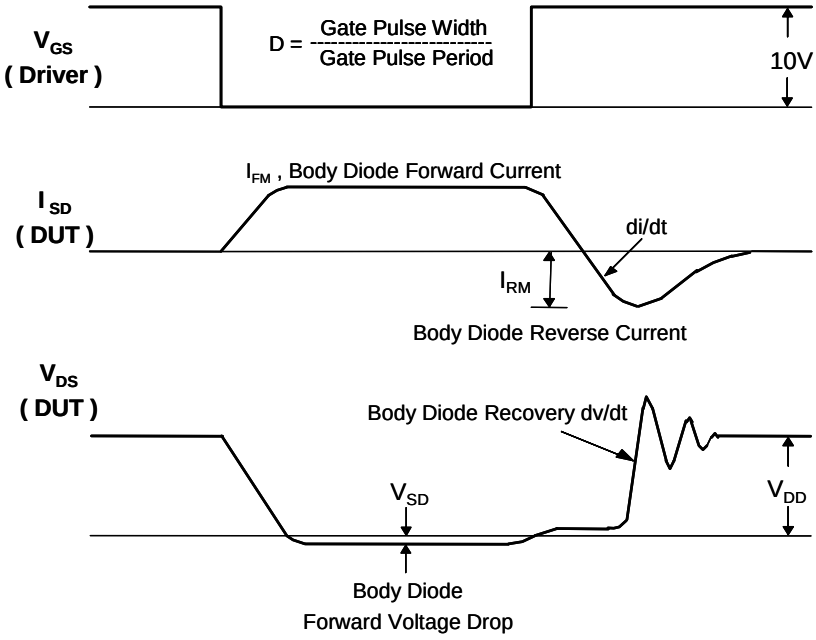


Unclamped Inductive Switching Test Circuit & Waveforms



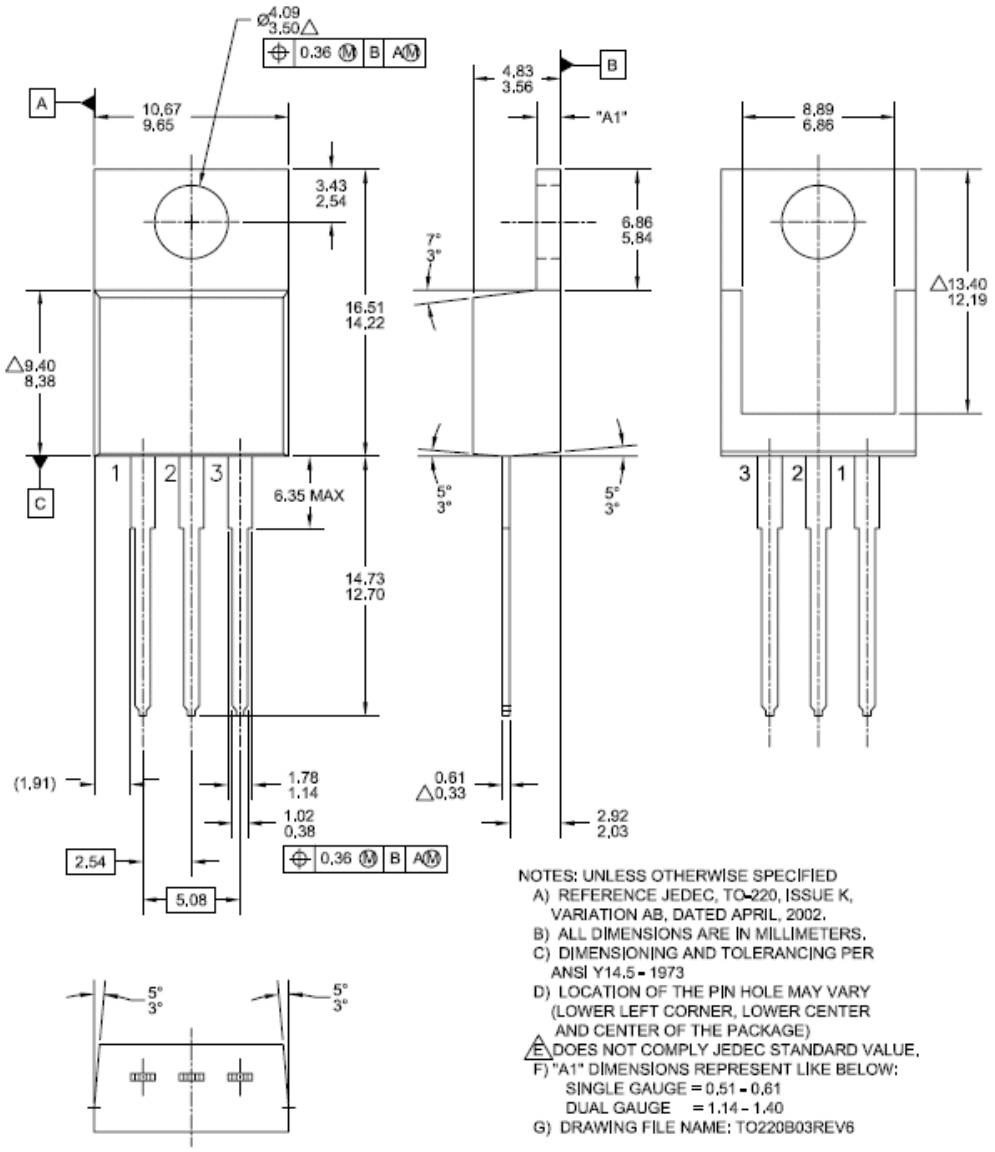
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Mechanical Dimensions

TO-220AB



NOTES: UNLESS OTHERWISE SPECIFIED
A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973
D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
△E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
SINGLE GAUGE = 0,51 - 0,61
DUAL GAUGE = 1.14 - 1.40
G) DRAWING FILE NAME: TO220B03REV6

Dimensions in Millimeters

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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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