

FDP085N10A_F102

N-Channel PowerTrench® MOSFET

100V, 96A, 8.5mΩ

Features

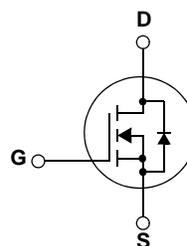
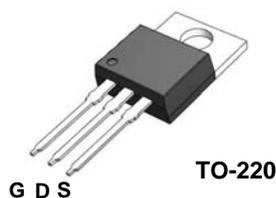
- $R_{DS(on)} = 7.35m\Omega$ (Typ.) @ $V_{GS} = 10V, I_D = 96A$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

- DC to DC Converters
- Synchronous Rectification for Telecommunication PSU
- Battery Charger
- AC motor drives and Uninterruptible Power Supplies
- Off-line UPS



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DSS}	Drain to Source Voltage	100	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	-Continuous ($T_C = 25^\circ C$)	96
		-Continuous ($T_C = 100^\circ C$)	68
I_{DM}	Drain Current	- Pulsed (Note 1)	384
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	269
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0
P_D	Power Dissipation	($T_C = 25^\circ C$)	188
		- Derate above $25^\circ C$	1.25
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ C$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ C$

Thermal Characteristics

Symbol	Parameter	Rated	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.8	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP085N10A	FDP085N10A_F102	TO-220	-	-	50

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_C = 25^\circ\text{C}$	100	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.07	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 80\text{V}, T_C = 150^\circ\text{C}$	-	-	1 500	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 96\text{A}$	-	7.35	8.5	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 96\text{A}$ (Note 4)	-	72	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	2025	2695	pF
C_{oss}	Output Capacitance		-	468	620	pF
C_{riss}	Reverse Transfer Capacitance		-	20	-	pF
$C_{oss(er)}$	Energy Releated Output Capacitance	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$	-	752	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{GS} = 10\text{V}, V_{DS} = 50\text{V}$ $I_D = 96\text{A}$	-	31	40	nC
Q_{gs}	Gate to Source Gate Charge		-	9.7	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	5.0	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4, 5)	-	7.5	-
ESR	Equivalent Series Resistance (G-S)	Drain Open, $f = 1\text{MHz}$	-	0.97	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{V}, I_D = 96\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 4.7\Omega$	-	18	46	ns
t_r	Turn-On Rise Time		-	22	54	ns
$t_{d(off)}$	Turn-Off Delay Time		-	29	68	ns
t_f	Turn-Off Fall Time		(Note 4, 5)	-	8	26

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	96	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	384	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 96\text{A}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$V_{DD} = 50\text{V}, V_{GS} = 0\text{V}, I_{SD} = 96\text{A}$	-	59	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$ (Note 4)	-	80	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 3\text{ mH}, I_{AS} = 13.4\text{ A}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 96\text{ A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Dual Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

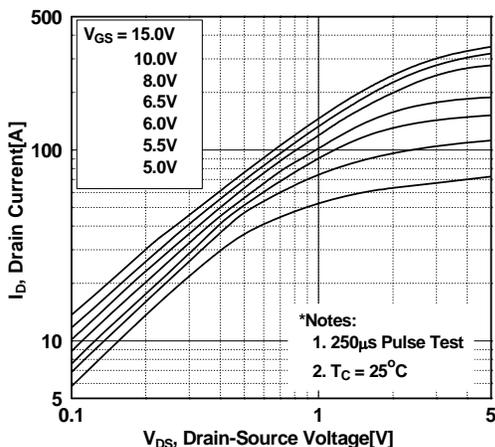


Figure 2. Transfer Characteristics

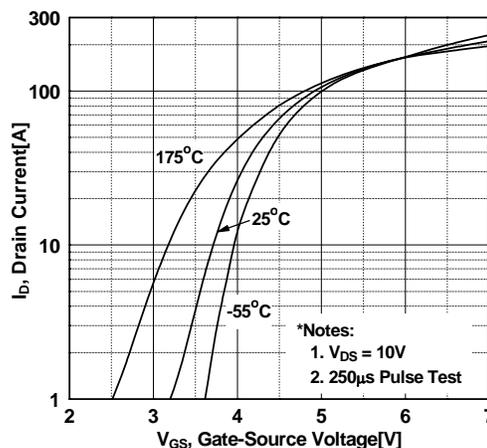


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

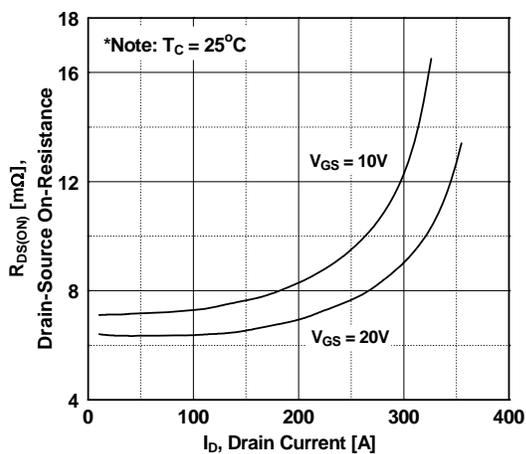


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

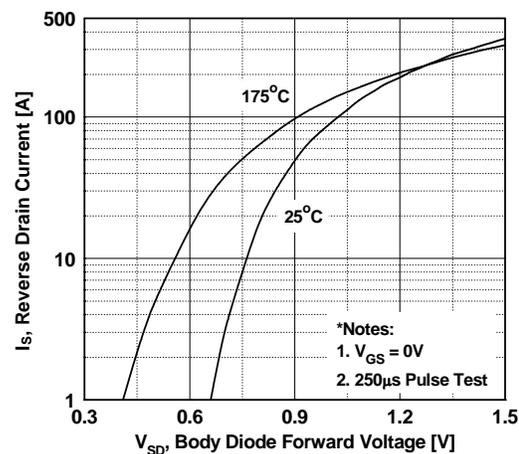


Figure 5. Capacitance Characteristics

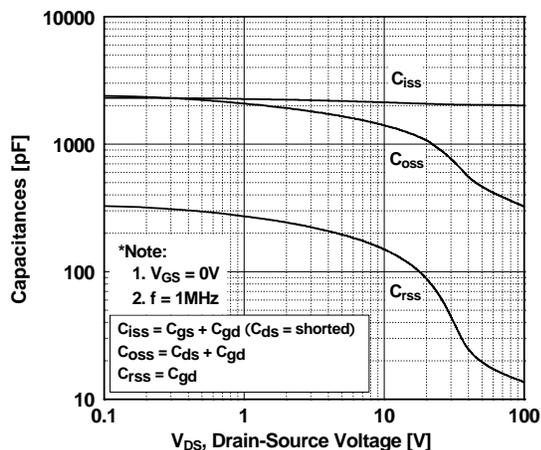
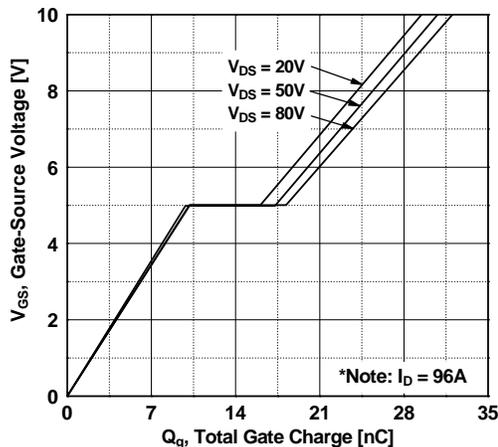


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

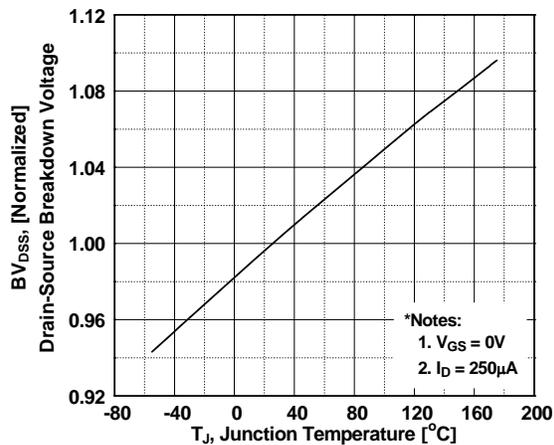


Figure 8. On-Resistance Variation vs. Temperature

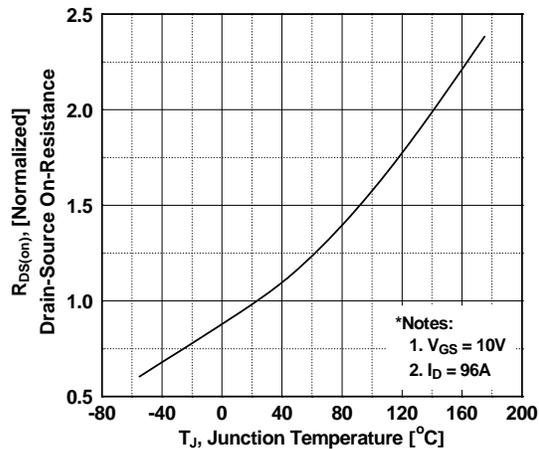


Figure 9. Maximum Safe Operating Area

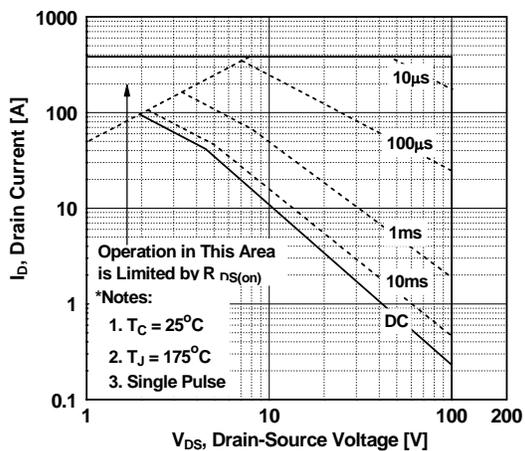


Figure 10. Maximum Drain Current vs. Case Temperature

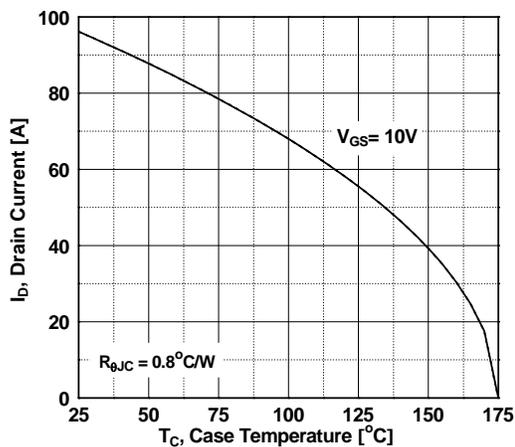


Figure 11. E_oss vs. Drain to Source Voltage

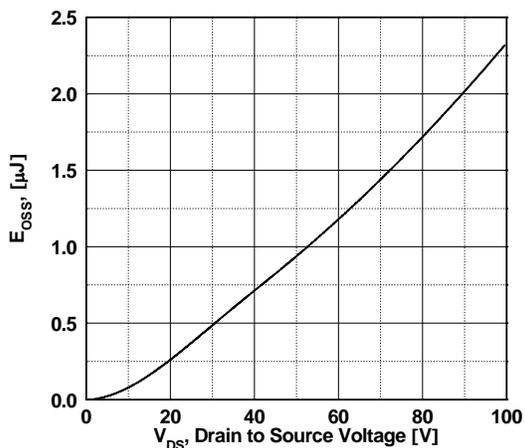
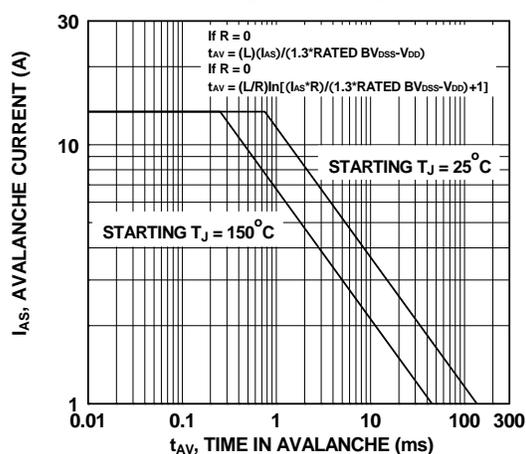
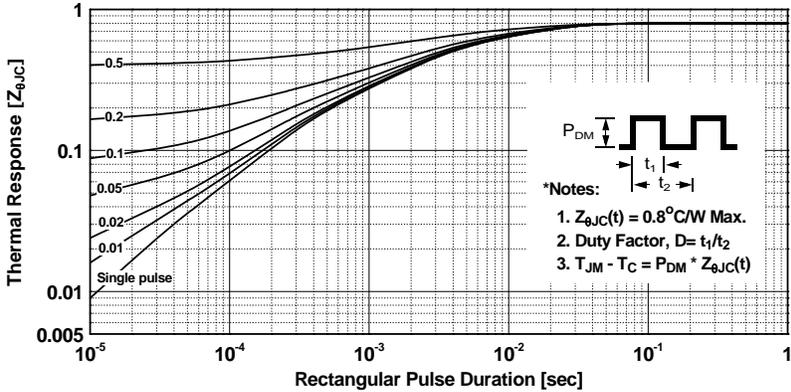


Figure 12. Unclamped Inductive Switching Capability

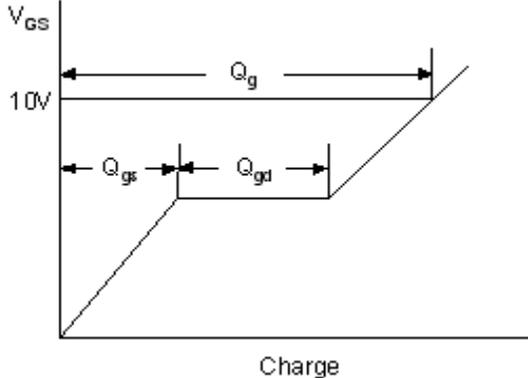
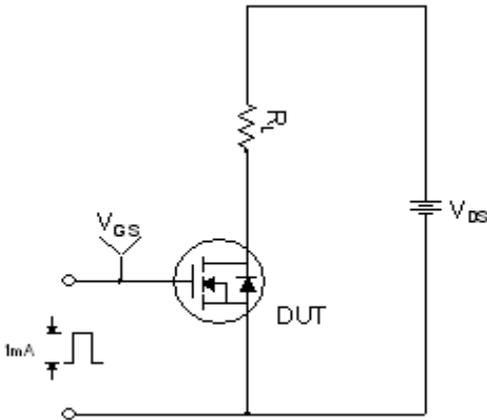


Typical Performance Characteristics (Continued)

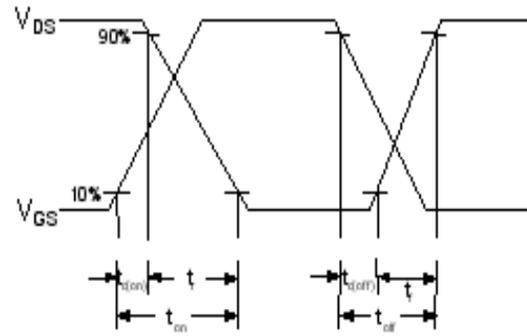
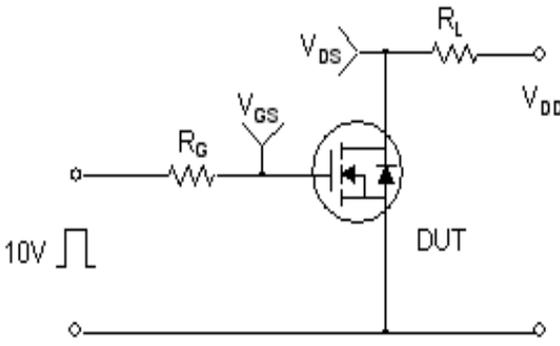
Figure 13. Transient Thermal Response Curve



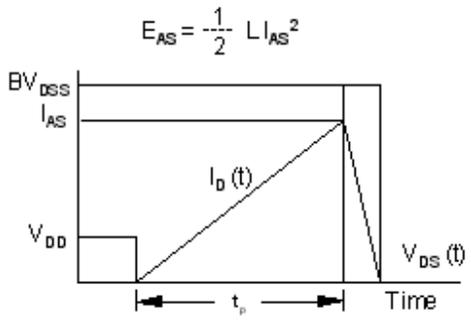
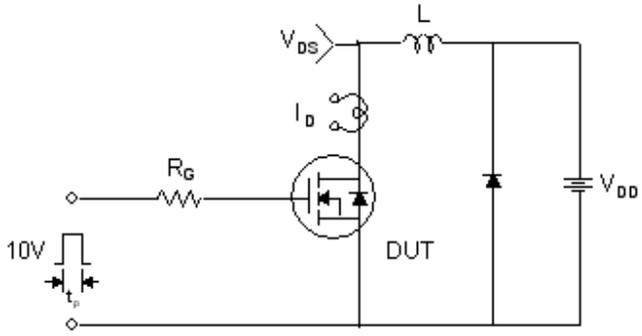
Gate Charge Test Circuit & Waveform



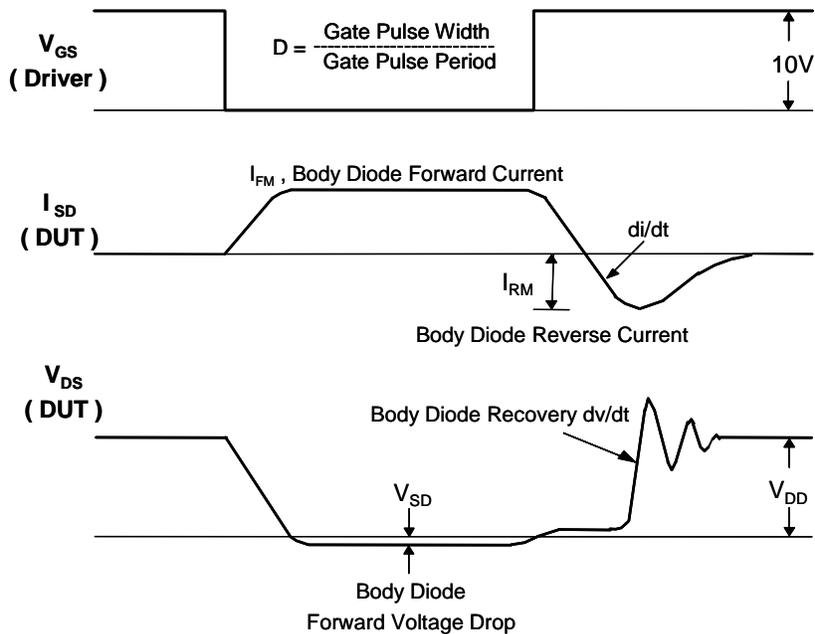
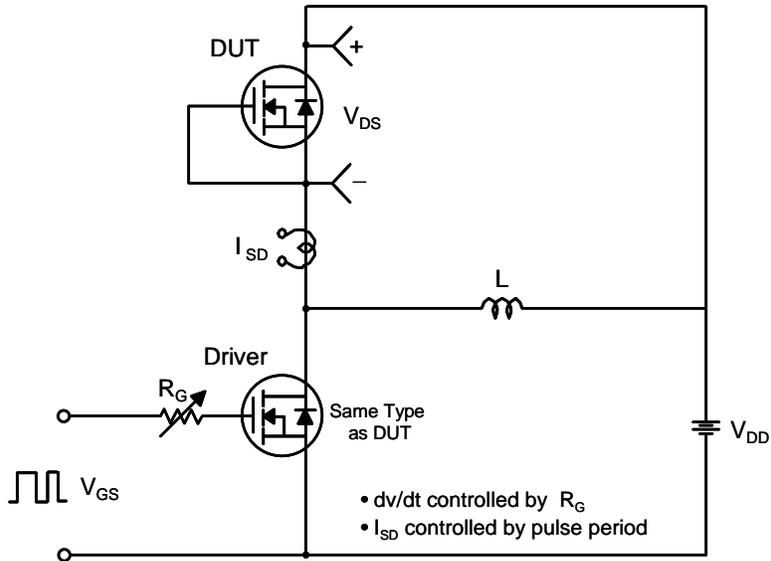
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

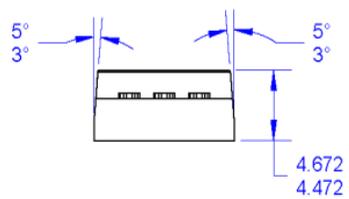
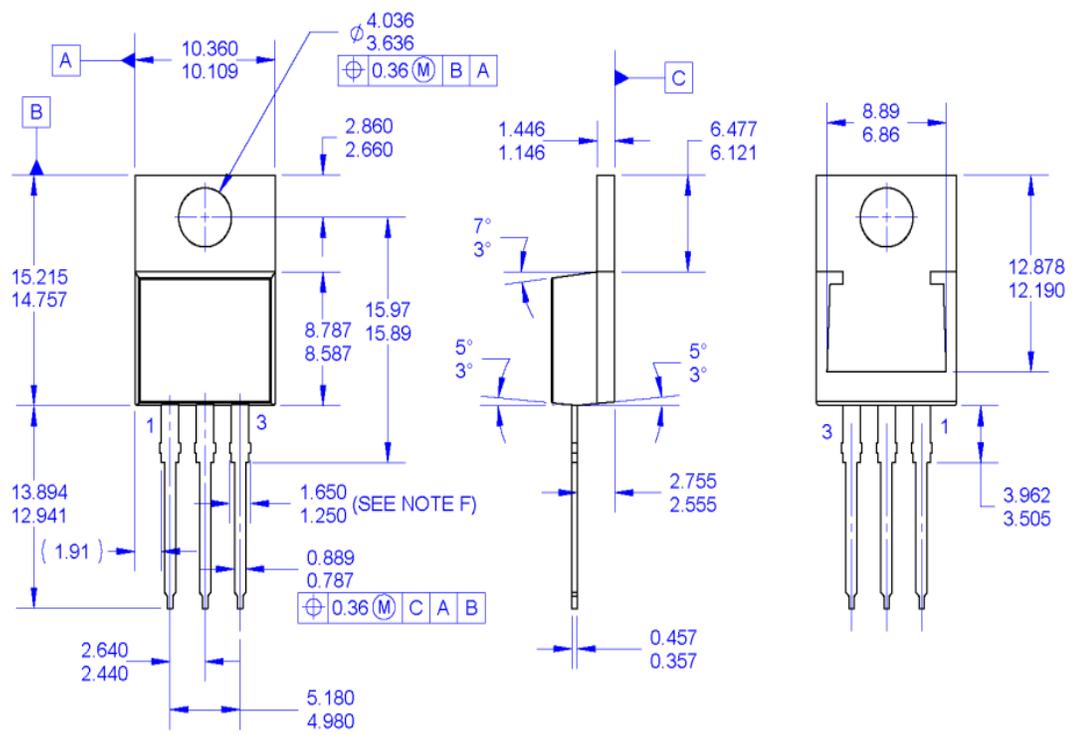


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

TO-220



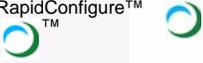
NOTES:

- A. PACKAGE REFERENCE: JEDEC TO220 VARIATION AB
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. THIS PACKAGE IS FSZZ INTERNAL PRODUCTION AND INTENDED FOR DELTA CUSTOMER ONLY.
- F. MAX WIDTH FOR F102 DEVICE = 1.35mm.
- G. DRAWING FILE NAME: TO220T03REV2



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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