

FDS6990A

Dual N-Channel Logic Level PowerTrench MOSFET

General Description

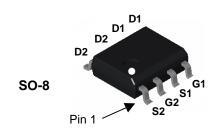
These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

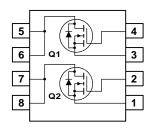
These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

• 7.5 A, 30 V. $R_{DS(ON)} = 18 \ m\Omega \ @ \ V_{GS} = 10 \ V$ $R_{DS(ON)} = 23 \ m\Omega \ @ \ V_{GS} = 4.5 \ V$

- · Fast switching speed
- · Low gate charge
- High performance trench technology for extremely low $R_{\mbox{\scriptsize DS(ON)}}$
- High power and current handling capability





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-Source Voltage		30	V
V _{GSS}	Gate-Source Voltage		± 20	V
I _D	Drain Current - Continuous	(Note 1a)	7.5	A
	- Pulsed		20	
P _D	Power Dissipation for Single Operation	(Note 1a)	1.6	W
		(Note 1b)	1.0	
		(Note 1c)	0.9	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6990A	FDS6990A	13"	12mm	2500 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics			I	l	ı
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_D = 250 \mu\text{A}$	30			V
<u>ΔBV_{DSS}</u> ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C		26		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			1 10	μΑ
I _{GSS}	Gate-Source Leakage	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA
On Char	acteristics (Note 2)					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C		-4		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$V_{GS} = 10 \text{ V}, I_D = 7.5 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 6.5 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 7.5 \text{ A}, T_J = 125^{\circ}\text{C}$		11 13 15	18 23 31	mΩ
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	20			Α
g fs	Forward Transconductance	$V_{DS} = 5 \text{ V}, \qquad I_{D} = 7.5 \text{ A}$		33		S
Dynamic	Characteristics	•	•	•		•
C _{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$		1235		pF
Coss	Output Capacitance	f = 1.0 MHz		295		pF
C _{rss}	Reverse Transfer Capacitance	7		120		pF
R _G	Gate Resistance	V _{GS} = 15 mV, f = 1.0 MHz		2.3		Ω
Switchin	g Characteristics (Note 2)	•				
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 15 \text{ V}, I_D = 1 \text{ A},$		10	19	ns
t _r	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$		5	10	ns
t _{d(off)}	Turn-Off Delay Time	7		28	44	ns
t _f	Turn-Off Fall Time	7		10	19	ns
Q _g	Total Gate Charge	$V_{DS} = 15 \text{ V}, I_{D} = 7.5 \text{ A},$		12	17	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 5 V		3.5		nC
Q_{gd}	Gate-Drain Charge			4.2		nC
Drain-Se	ource Diode Characteristics	and Maximum Ratings				
Is	Maximum Continuous Drain-Source				1.3	Α
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 1.3 \text{ A} \text{(Note 2)}$		0.7	1.2	V
t _{rr}	Diode Reverse Recovery Time	$I_F = 7.5 \text{ A}, d_{iF}/d_t = 100 \text{ A/}\mu\text{s}$		24		nS
Qrr	Diode Reverse Recovery Charge			13		nC

Notes

R_{8JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{8JC} is guaranteed by design while R_{8CA} is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum mounting pad.

Scale 1:1 on letter size paper

Pulse Test: Pulse Width < $300\mu s$, Duty Cycle < 2.0%

Typical Characteristics

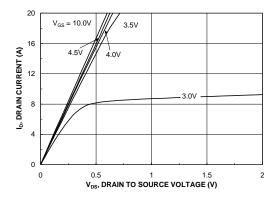


Figure 1. On-Region Characteristics.

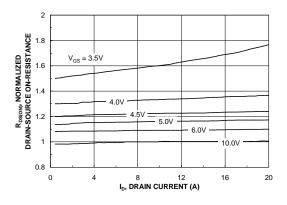


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

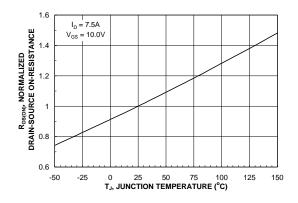


Figure 3. On-Resistance Variation with Temperature.

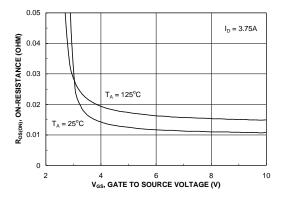


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

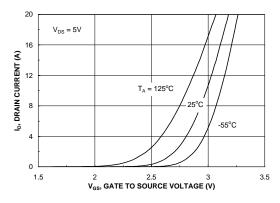


Figure 5. Transfer Characteristics.

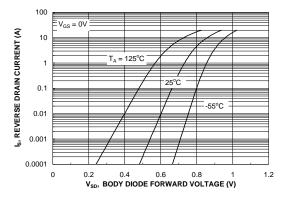
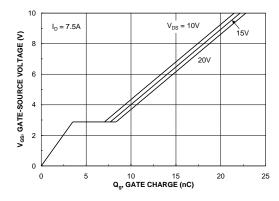


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics



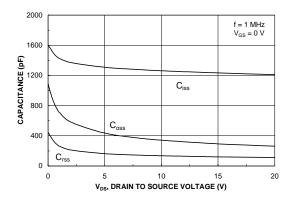
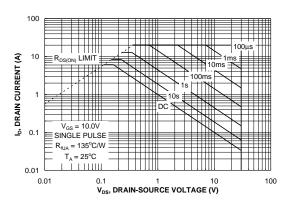


Figure 7. Gate Charge Characteristics.





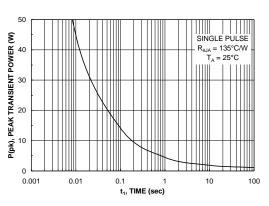


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

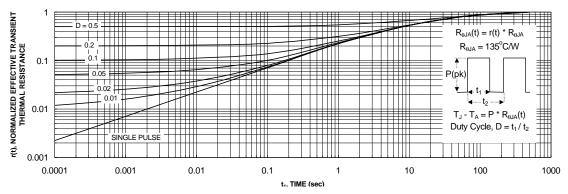


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

FACT Quiet Series™ LittleFET™ ACEx™ Power247™ SuperSOT™-6 MICROCOUPLER™ PowerTrench® ActiveArray™ SuperSOT™-8 FAST® Bottomless™ MicroFET™ **OFET®** SvncFET™ FASTr™ CoolFET™ QSTM TinyLogic[®] $\mathsf{FRFET}^\mathsf{TM}$ MicroPak™ CROSSVOLT™ MICROWIRE™ QT Optoelectronics™ TINYOPTO™ GlobalOptoisolator™ TruTranslation™ DOME™ GTO™ Quiet Series™ MSX™ UHC™ EcoSPARK™ RapidConfigure™ HiSeC™ MSXPro™ UltraFET® E²CMOSTM I2CTM OCX^{TM} RapidConnect™ EnSigna™ SILENT SWITCHER® VCX^{TM} ImpliedDisconnect[™] OCXPro[™] FACT™ OPTOLOGIC® SMART START™ ISOPLANAR™ SPM™ Across the board. Around the world. $^{\text{TM}}$ OPTOPLANAR $^{\text{TM}}$ Stealth™ PACMAN™ The Power Franchise™ РОРТМ SuperSOT™-3

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS. NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

Programmable Active Droop™

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.