FAIRCHILD

SEMICONDUCTOR ™

April 2000

QFET™

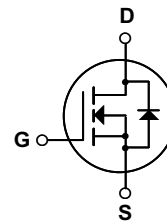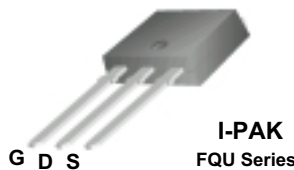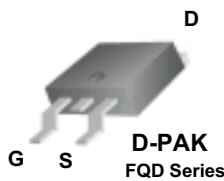# FQD7N30 / FQU7N30

300V N-Channel MOSFET

General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supply.

Features

- 5.5A, 300V, $R_{DS(on)}$ = 0.7Ω @V_{GS} = 10 V
- Low gate charge (typical 13 nC)
- Low Crss (typical 12 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

D-PAK
FQD Series

G S

I-PAK
FQU Series

G D S

D

G

S

Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter			FQD7N30 / FQU7N30	Units
V_{DSS}	Drain-Source Voltage			300	V
I_D	Drain Current	- Continuous (T_C = 25°C)		5.5	A
		- Continuous (T_C = 100°C)		3.48	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	22	A
V_{GSS}	Gate-Source Voltage			± 30	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	380	mJ
I_{AR}	Avalanche Current		(Note 1)	5.5	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *			2.5	W
	Power Dissipation (T_C = 25°C)			50	W
	- Derate above 25°C			0.4	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds			300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_C = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ μA	300	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	$I_D = 250$ μA, Referenced to 25°C	--	0.3	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 300$ V, $V_{GS} = 0$ V	--	--	1	μA
		$V_{DS} = 240$ V, $T_C = 125°C$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30$ V, $V_{DS} = 0$ V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30$ V, $V_{DS} = 0$ V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ μA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 2.75$ A	--	0.53	0.7	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50$ V, $I_D = 2.75$ A (Note 4)	--	4.0	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1.0 MHz	--	470	610	pF
C_{oss}	Output Capacitance		--	100	130	pF
C_{rss}	Reverse Transfer Capacitance		--	12	16	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 150$ V, $I_D = 7.0$ A, $R_G = 25$ Ω	--	13	35	ns
t_r	Turn-On Rise Time		--	75	160	ns
$t_{d(off)}$	Turn-Off Delay Time		--	25	60	ns
t_f	Turn-Off Fall Time	(Note 4, 5)	--	35	80	ns
Q_g	Total Gate Charge	$V_{DS} = 240$ V, $I_D = 7.0$ A, $V_{GS} = 10$ V	--	13	17	nC
Q_{gs}	Gate-Source Charge		--	3.4	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)	--	6.4	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	5.5	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	22	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 5.5$ A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0$ V, $I_S = 7.0$ A, $dI_F / dt = 100$ A/μs (Note 4)	--	150	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.74	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 21mH, I_{AS} = 5.5A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 7.0A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature
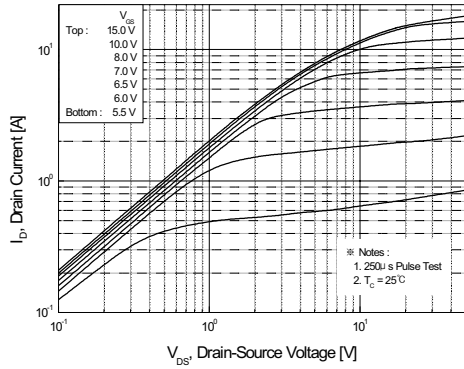
Typical Characteristics
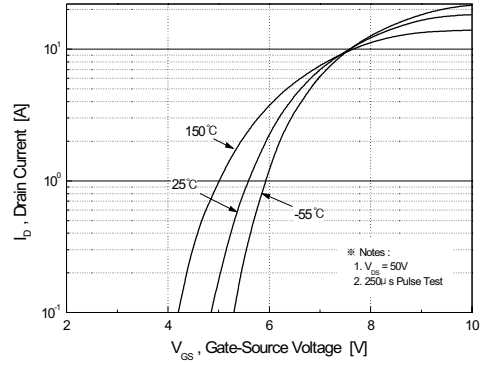

Figure 1. On-Region Characteristics

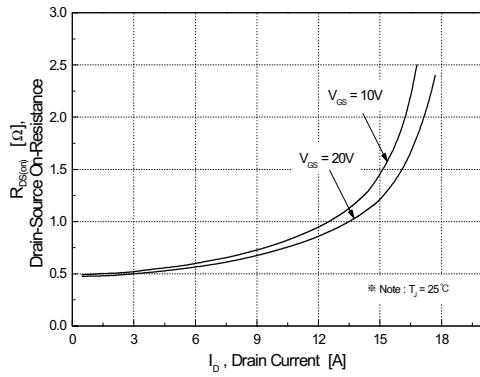**Figure 2. Transfer Characteristics**

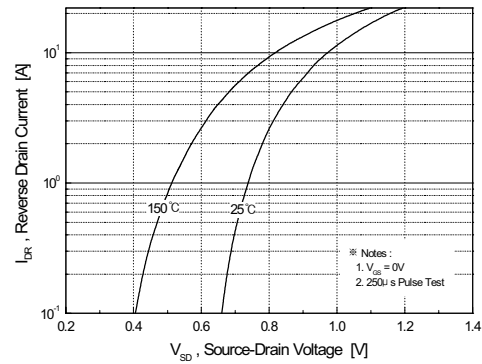**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature
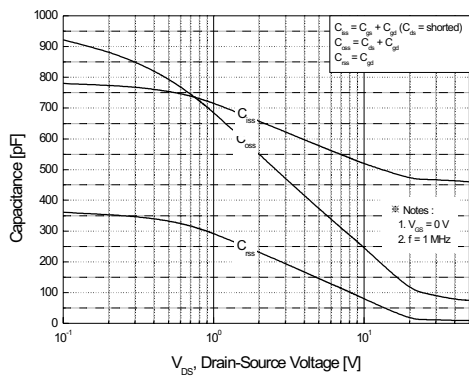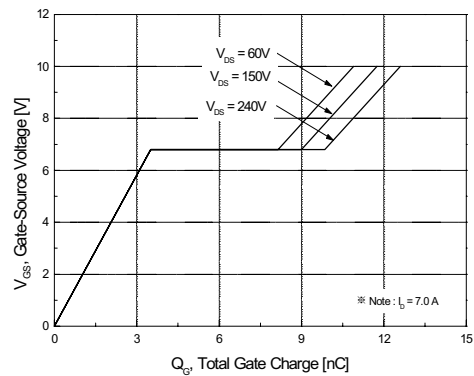

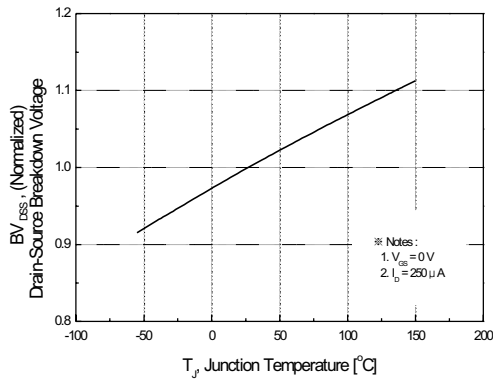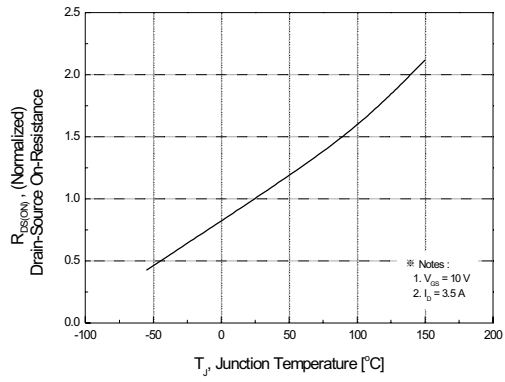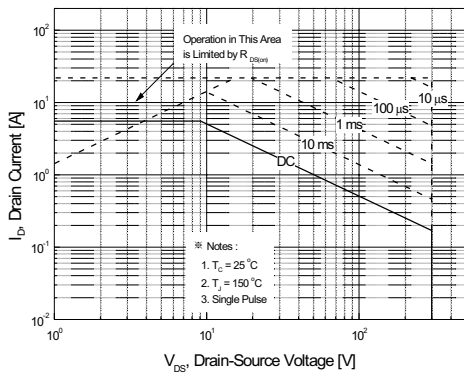**Figure 5. Capacitance Characteristics**

Figure 6. Gate Charge Characteristics
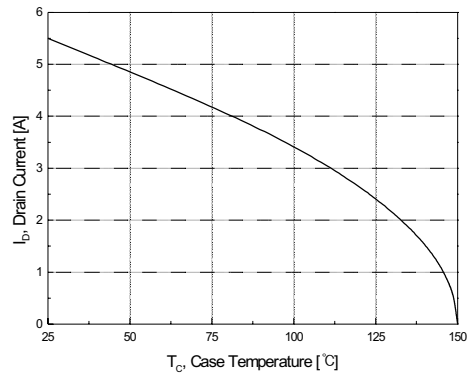
Typical Characteristics (Continued)

BV$_{DSS}$, (Normalized) Drain-Source Breakdown Voltage

T$_J$, Junction Temperature [°C]

※ Notes :
1. V$_{GS}$ = 0 V
2. I$_D$ = 250 μA

Figure 7. Breakdown Voltage Variation vs. Temperature

R$_{DS(ON)}$, (Normalized) Drain-Source On-Resistance

T$_J$, Junction Temperature [°C]

※ Notes :
1. V$_{GS}$ = 10 V
2. I$_D$ = 3.5 A

Figure 8. On-Resistance Variation vs. Temperature

I$_D$, Drain Current [A]

Operation in This Area is Limited by R$_{DS(on)}$

10 μs
100 μs
1 ms
10 ms
DC

V$_{DS}$, Drain-Source Voltage [V]

※ Notes :
1. T$_C$ = 25 °C
2. T$_J$ = 150 °C
3. Single Pulse

Figure 9. Maximum Safe Operating Area

I$_D$, Drain Current [A]

T$_C$, Case Temperature [°C]

Figure 10. Maximum Drain Current vs. Case Temperature

Z$_{\theta JC}$(t), Thermal Response

D = 0.5
0.2
0.1
0.05
0.02
0.01
single pulse

※ Notes :
1. Z$_{\theta JC}$(t) = 2.5 °C /W Max.
2. Duty Factor, D = t$_1$/t$_2$
3. T$_{JM}$ - T$_C$ = P$_{DM}$ • Z$_{\theta JC}$(t)

P$_{DM}$
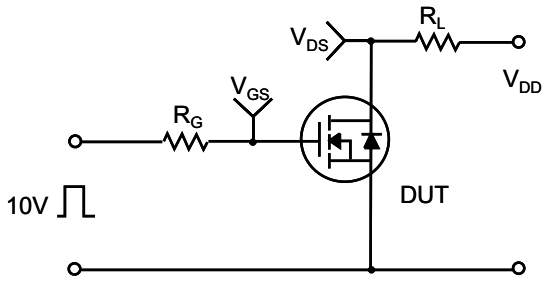t$_1$
t$_2$

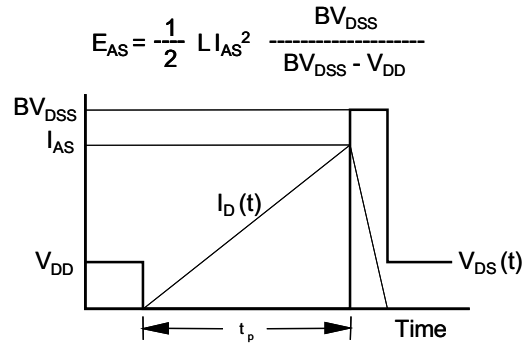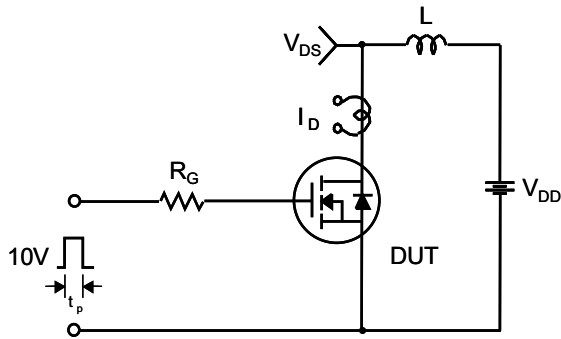t$_1$, Square Wave Pulse Duration [sec]
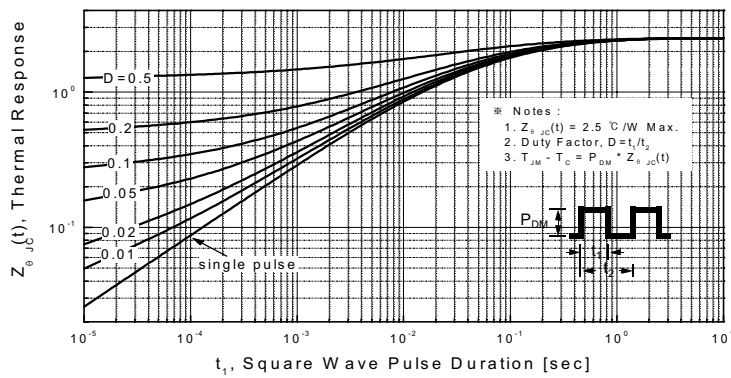
Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform

12V | 200nF | 50KΩ | 300nF
V_{GS}
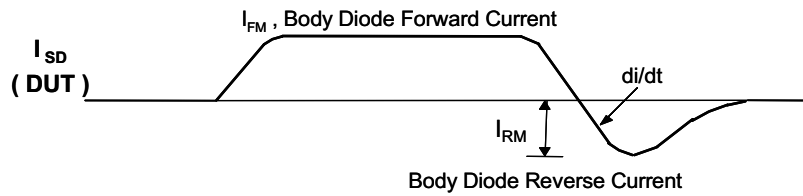3mA

Same Type as DUT
DUT
V_{DS}

V_{GS}
10V
Q_g
Q_{gs} | Q_{gd}
Charge

Resistive Switching Test Circuit & Waveforms

R_G | V_{GS} | V_{DS} | R_L | V_{DD}
10V
DUT

V_{DS}
90%
V_{GS}
10%
$t_{d(on)}$ | t_r | $t_{d(off)}$ | t_f
t_{on} | t_{off}
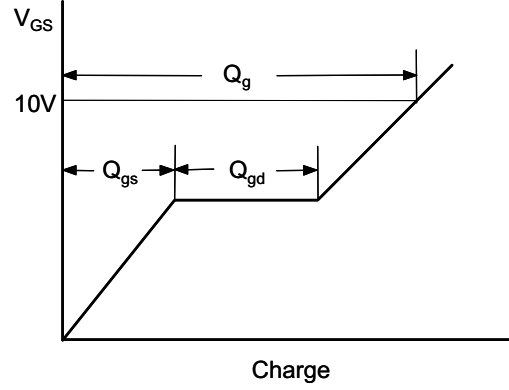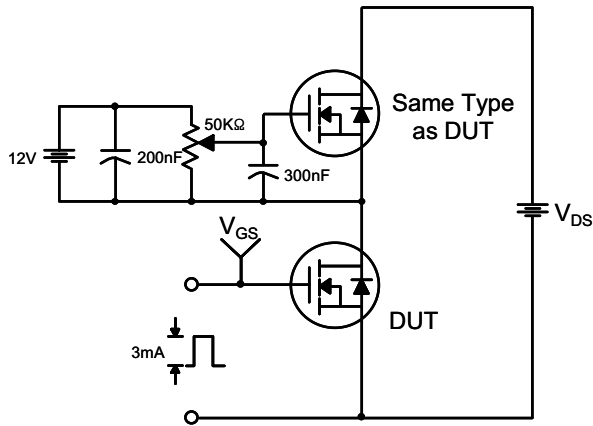
Unclamped Inductive Switching Test Circuit & Waveforms

V_{DS} | L
I_D
R_G
10V
t_p
DUT
V_{DD}

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \; \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

BV_{DSS}
I_{AS}
$I_D(t)$
V_{DD}
$V_{DS}(t)$
t_p
Time

Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

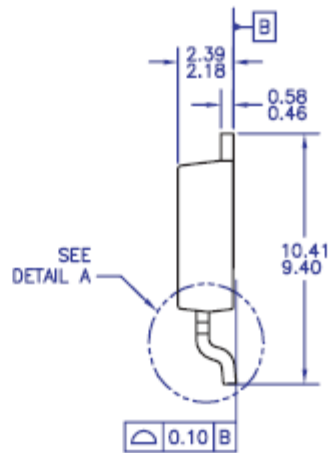$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop

Package Dimensions

D - PAK

LAND PATTERN RECOMMENDATION

SEE NOTE D

SEE DETAIL A

GAGE PLANE

DETAIL A
(ROTATED −90°)
SCALE: 12X
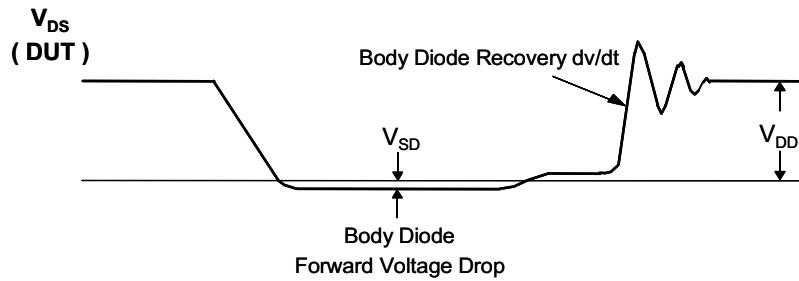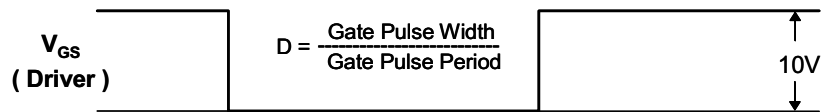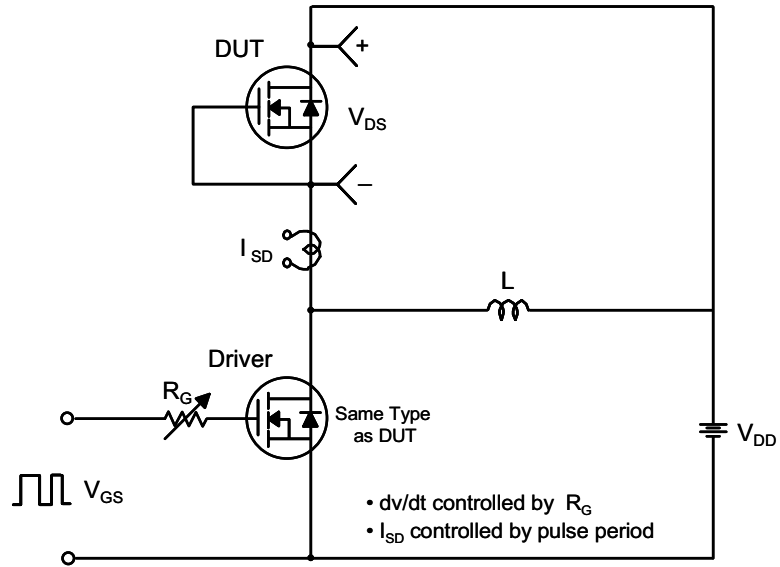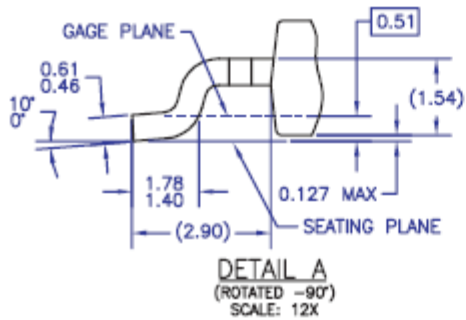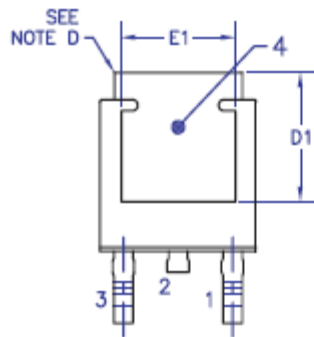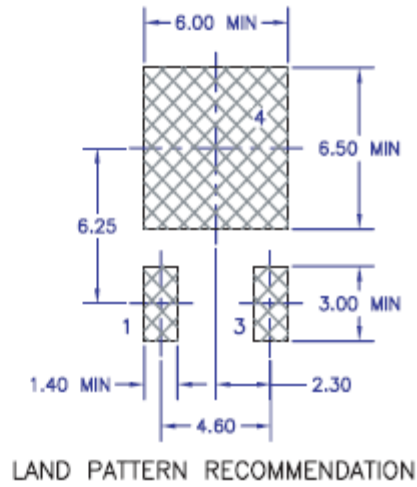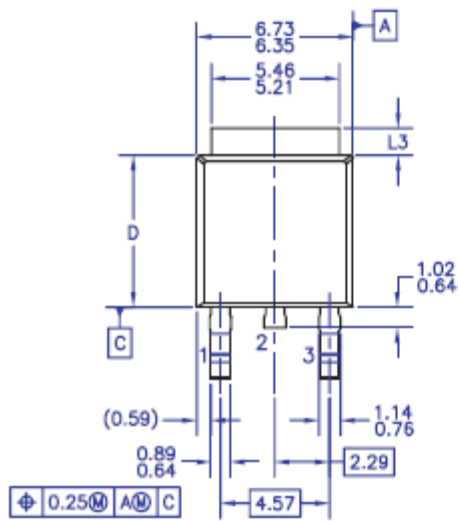
Dimensions in Millimeters

Package Dimensions (Continued)

I - PAK

Dimensions in Millimeters

TRADEMARKS

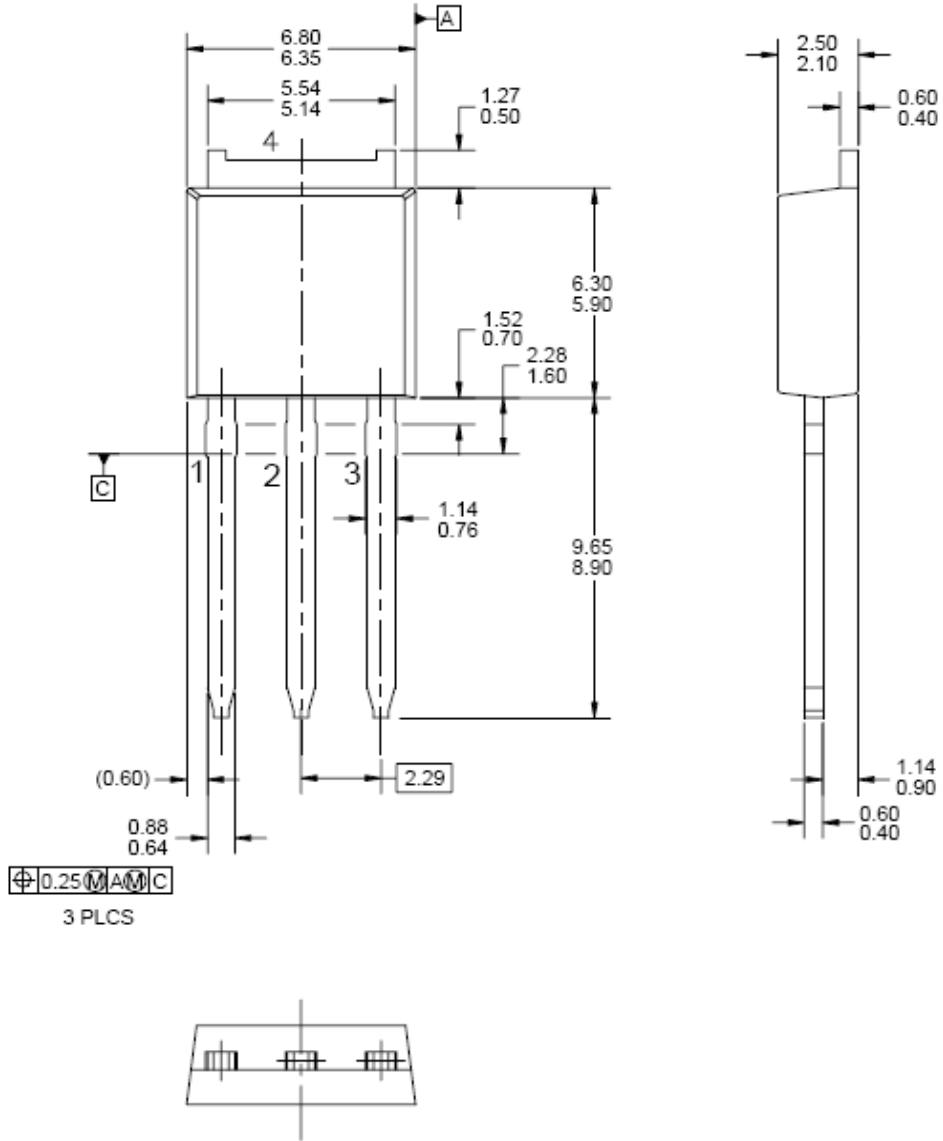The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	HiSeC™	SuperSOT™-8
Bottomless™	ISOPLANAR™	SyncFET™
CoolFET™	MICROWIRE™	TinyLogic™
CROSSVOLT™	POP™	UHC™
E^{2}CMOS™	PowerTrench$^®$	VCX™
FACT™	QFET™	
FACT Quiet Series™	QS™	
FAST$^®$	Quiet Series™	
FASTr™	SuperSOT™-3	
GTO™	SuperSOT™-6	

DISCLAIMER
FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR INTERNATIONAL.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.