HARRIS HGTG20N100D2

May 1995

HGTG20N100D2

20A, 1000V N-Channel IGBT

HGTG20N100D2

Features Package • 34A, 1000V **JEDEC STYLE TO-247** EMITTER Latch Free Operation COLLECTOR Typical Fall Time 520ns GATE · High Input Impedance Low Conduction Loss COLLECTOR (BOTTOM SIDE METAL) (III) Description The HGTG20N100D2 is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOS-FET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately **Terminal Diagram** between +25°C and +150°C. N-CHANNEL ENHANCEMENT MODE IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors. PACKAGING AVAILABILITY PART NUMBER PACKAGE BRAND

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

G20N100D2

TO-247

	HGIGZUNTUUDZ	UNITS
Collector-Emitter Voltage BV _{CES}	1000	V
Collector-Gate Voltage $R_{GE} = 1M\Omega$ BV_{CGR}	1000	V
Collector Current Continuous at $T_c = +25^{\circ}C$ I_{c25}	34	А
at $T_{C} = +90^{\circ}C$ I_{C90}	20	А
Collector Current Pulsed (Note 1)ICM	100	А
Gate-Emitter Voltage Continuous.	±20	V
Gate-Emitter Voltage Pulsed	±30	V
Switching Safe Operating Area at T _J = +150°CSSOA	100A at 0.8 BV _{CES}	-
Power Dissipation Total at $T_{C} = +25^{\circ}C$ P_{D}	150	W
Power Dissipation Derating T _C > +25°C	1.20	W/ºC
Operating and Storage Junction Temperature Range	-55 to +150	°C
Maximum Lead Temperature for SolderingT _L (0.125 inch from case for 5 seconds)	260	°C
Short Circuit Withstand Time (Note 2) at V _{GE} = 15Vt _{SC}	3	μs
at V _{GE} = 10Vt _{SC}	15	μs
NOTES:		
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1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. $V_{CE(PEAK)} = 600V$, $T_C = +125^{\circ}C$, $R_{GE} = 25\Omega$.

HARRIS S	EMICONDUCTO	R IGBT PRODU	CT IS COVERED	BY ONE OR MO	ORE OF THE FO	LLOWING U.S. F	PATENTS:
4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures. Copyright © Harris Corporation 1995

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		TEST CONDITIONS $I_{C} = 250 \text{mA}, V_{GE} = 0 \text{V}$		LIMITS			
PARAMETERS	SYMBOL BV _{CES}			MIN 1000	TYP -	MAX -	UNITS V
Collector-Emitter Breakdown Voltage							
Collector-Emitter Leakage Voltage	I _{CES}	$V_{CE} = BV_{CES}$	T _C = +25°C	-	-	250	μΑ
		$V_{CE} = 0.8 \text{ BV}_{CES}$	T _C = +125 ^o C	-	-	1.0	mA
Collector-Emitter Saturation Voltage	$\frac{V_{CE(SAT)}}{I_{C} = I_{C90},} \\ \frac{V_{GE} = 15V}{I_{C} = I_{C90},} \\ \frac{V_{GE} = 10V}{V_{GE} = 10V}$		$T_{C} = +25^{\circ}C$	-	3.1	3.8	V
		V _{GE} = 15V	T _C = +125°C	-	2.9	3.6	V
		$I_{C} = I_{C90},$ $V_{GE} = 10V$	T _C = +25 ^o C	-	3.3	4.1	V
			T _C = +125°C	-	3.2	4.0	V
Gate-Emitter Threshold Voltage	V _{GE(TH)}	$I_{C} = 500\mu A,$ $V_{CE} = V_{GE}$	T _C = +25°C	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I _{GES}	$V_{GE} = \pm 20 V$		-	-	±250	nA
Gate-Emitter Plateau Voltage	V _{GEP}	$I_{C} = I_{C90}, V_{CE} = 0.5 \text{ BV}_{CES}$		-	7.1	-	V
On-State Gate Charge	Q _{G(ON)}	$I_{C} = I_{C90},$ $V_{CE} = 0.5 \text{ BV}_{CES}$	V _{GE} = 15V	-	120	160	nC
			V _{GE} = 20V	-	163	212	nC
Current Turn-On Delay Time	t _{D(ON)}	$\label{eq:linear} \begin{array}{l} {\sf L} = 50 \mu {\sf H}, {\sf I}_{{\sf C}} = {\sf I}_{{\sf C90}}, {\sf R}_{{\sf G}} = 25 \Omega, \\ {\sf V}_{{\sf GE}} = 15 {\sf V}, {\sf T}_{{\sf J}} = +125^{\circ} {\sf C}, \\ {\sf V}_{{\sf CE}} = 0.8 \; {\sf BV}_{{\sf CES}} \end{array}$		-	100	-	ns
Current Rise Time	t _{RI}			-	150	-	ns
Current Turn-Off Delay Time	t _{D(OFF)} I			-	500	650	ns
Current Fall Time	t _{FI}			-	520	680	ns
Turn-Off Energy (Note 1)	W _{OFF}	1	-	3.7	-	mJ	
Current Turn-On Delay Time	t _{D(ON)}	$\label{eq:L} \begin{array}{l} {\sf L} = 50 \mu {\sf H}, \; {\sf I}_{{\sf C}} = {\sf I}_{{\sf C}90}, \; {\sf R}_{{\sf G}} = 25 \Omega, \\ {\sf V}_{{\sf GE}} = 10 {\sf V}, \; {\sf T}_{{\sf J}} = +125^{\circ} {\sf C}, \\ {\sf V}_{{\sf CE}} = 0.8 \; {\sf BV}_{{\sf CES}} \end{array}$		-	100	-	ns
Current Rise Time	t _{RI}			-	150	-	ns
Current Turn-Off	t _{D(OFF)} I			-	410	530	ns
Current Fall Time	t _{FI}	1	-	520	680	ns	
Turn-Off Energy (Note 1)	W _{OFF}	1	-	3.7	-	mJ	
Thermal Resistance	$R_{ extsf{ heta}JC}$			-	0.7	0.83	°C/W

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

NOTE: 1. Turn-Off Energy Loss (W_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($_{CE}$ = 0A) The HGTG20N100D2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves









Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

 f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the onstate time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device

turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX} . $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

 f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/W_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D . A 50% duty factor was used (Figure 10) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \bullet I_{CE})/2$. W_{OFF} is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$).

The switching power loss (Figure 10) is defined as $f_{MAX2} \bullet W_{OFF}.$ Turn-on switching losses are not included because they can be greatly influenced by external circuit conditions and components.