

40A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode

January 1996

Features

- 40A, 600V at $T_C = +25^\circ\text{C}$
- Typical Fall Time - 140ns at $+150^\circ\text{C}$
- Short Circuit Rated
- Low Conduction Loss
- Hyperfast Anti-Parallel Diode

Description

The HGTG20N60B3D is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between $+25^\circ\text{C}$ and $+150^\circ\text{C}$. The diode used in anti-parallel with the IGBT is the RHRP3060.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential.

PACKAGING AVAILABILITY

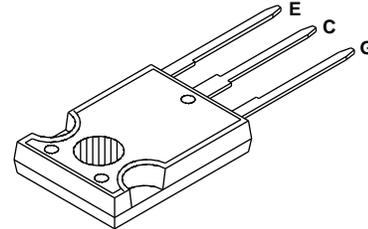
PART NUMBER	PACKAGE	BRAND
HGTG20N60B3D	TO-247	G20N60B3D

NOTE: When ordering, use the entire part number.

Formerly Developmental Type TA49016.

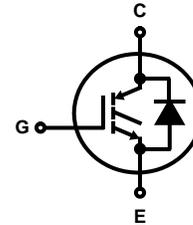
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

	HGTG20N60B3D	UNITS
Collector-Emitter Voltage	600	V
Collector-Gate Voltage, $R_{GE} = 1\text{M}\Omega$	600	V
Collector Current Continuous		
At $T_C = +25^\circ\text{C}$	40	A
At $T_C = +110^\circ\text{C}$	20	A
Average Diode Forward Current at $+110^\circ\text{C}$	20	A
Collector Current Pulsed (Note 1)	160	A
Gate-Emitter Voltage Continuous	± 20	V
Gate-Emitter Voltage Pulsed	± 30	V
Switching Safe Operating Area at $T_C = +150^\circ\text{C}$	80A at $0.8 BV_{CES}$	
Power Dissipation Total at $T_C = +25^\circ\text{C}$	165	W
Power Dissipation Derating $T_C > +25^\circ\text{C}$	1.32	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	-40 to +150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering	260	$^\circ\text{C}$
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15\text{V}$	4	μs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10\text{V}$	10	μs

NOTE:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360\text{V}$, $T_C = +125^\circ\text{C}$, $R_{GE} = 25\Omega$.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

Specifications HGTG20N60B3D

Electrical Specifications $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu\text{A}$, $V_{GE} = 0\text{V}$	600	-	-	V	
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$, $T_C = +25^\circ\text{C}$	-	-	250	μA	
		$V_{CE} = BV_{CES}$, $T_C = +150^\circ\text{C}$	-	-	2.0	mA	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15\text{V}$	$T_C = +25^\circ\text{C}$	-	1.8	2.0	V
			$T_C = +150^\circ\text{C}$	-	2.1	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu\text{A}$, $V_{CE} = V_{GE}$	$T_C = +25^\circ\text{C}$	3.0	5.0	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20\text{V}$	-	-	± 100	nA	
Latching Current	I_L	$T_C = +150^\circ\text{C}$, $V_{CE(PK)} = 0.8 BV_{CES}$, $V_{GE} = 15\text{V}$, $R_G = 10\Omega$, $L = 45\mu\text{H}$	80	-	-	A	
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5 BV_{CES}$	-	8.0	-	V	
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5 BV_{CES}$	$V_{GE} = 15\text{V}$	-	80	105	nC
			$V_{GE} = 20\text{V}$	-	105	135	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_C = +150^\circ\text{C}$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8 BV_{CES}$, $V_{GE} = 15\text{V}$, $R_G = 10\Omega$, $L = 100\mu\text{H}$	-	25	-	ns	
Current Rise Time	t_{RI}		-	20	-	ns	
Current Turn-Off Delay Time	$t_{D(OFF)I}$		-	220	275	ns	
Current Fall Time	t_{FI}		-	140	200	ns	
Turn-On Energy	E_{ON}		-	475	-	μJ	
Turn-Off Energy (Note 1)	E_{OFF}		-	1050	-	μJ	
Diode Forward Voltage	V_{EC}		$I_{EC} = 20\text{A}$	-	1.5	1.9	V
Diode Reverse Recovery Time	t_{RR}	$I_{EC} = 20\text{A}$, $dI_{EC}/dt = 100\text{A}/\mu\text{s}$	-	-	55	ns	
		$I_{EC} = 1\text{A}$, $dI_{EC}/dt = 100\text{A}/\mu\text{s}$	-	-	45	ns	
Thermal Resistance	$R_{\theta JC}$	IGBT	-	-	0.76	$^\circ\text{C}/\text{W}$	
		Diode	-	-	1.2	$^\circ\text{C}/\text{W}$	

NOTE:

- Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0\text{A}$). The HGTG20N60B3D was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include diode losses.

Typical Performance Curves

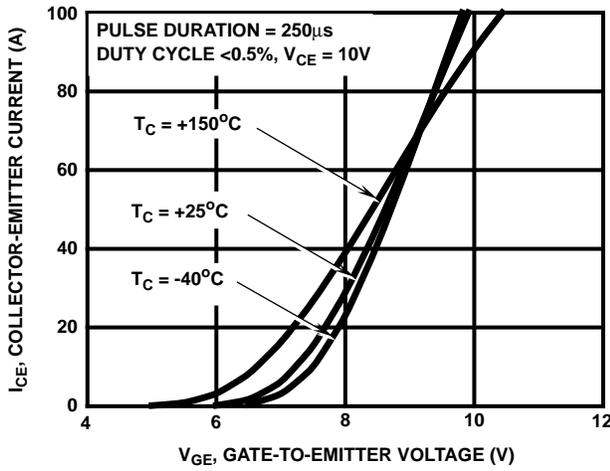


FIGURE 1. TRANSFER CHARACTERISTICS

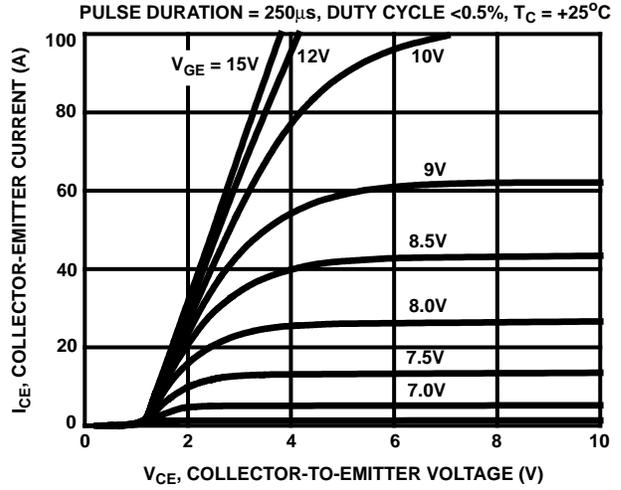


FIGURE 2. SATURATION CHARACTERISTICS

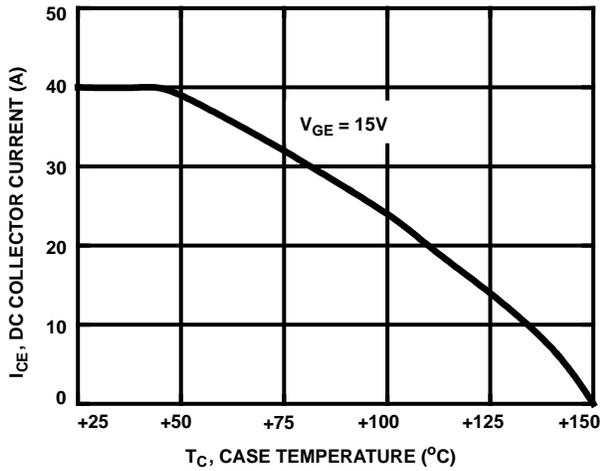


FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

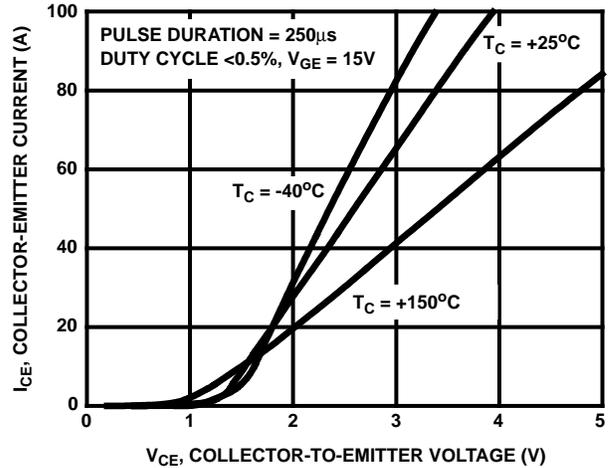


FIGURE 4. COLLECTOR-EMITTER ON-STATE VOLTAGE

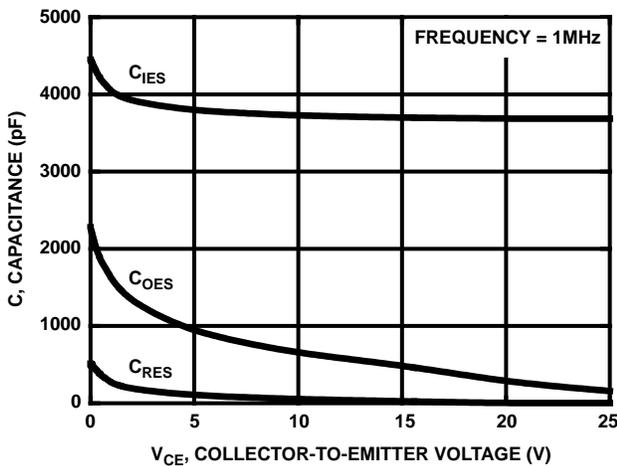


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

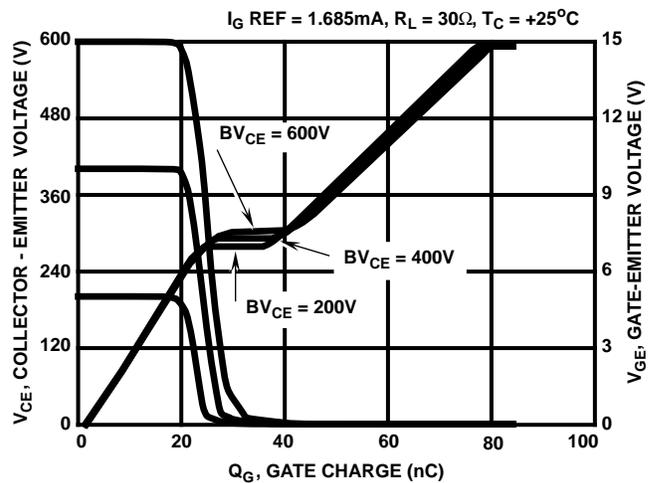


FIGURE 6. GATE CHARGE WAVEFORMS

Typical Performance Curves (Continued)

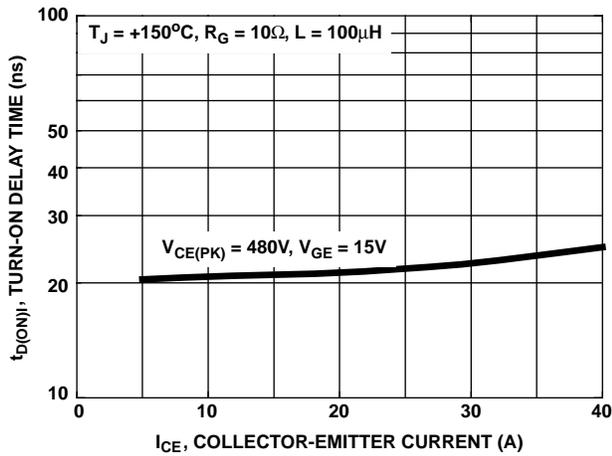


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

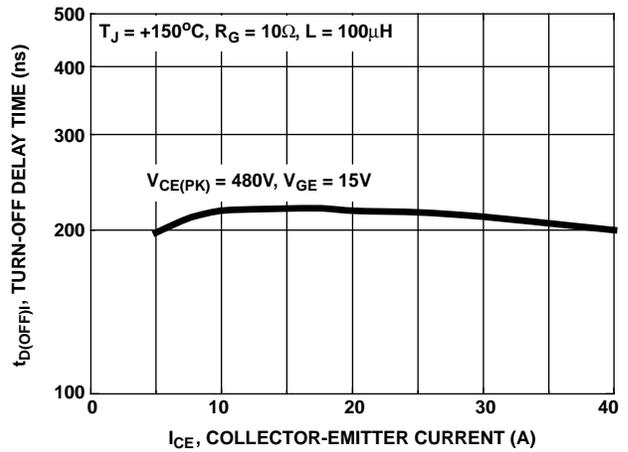


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

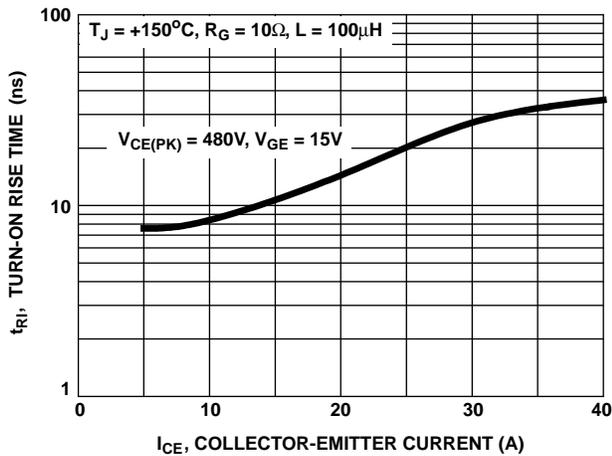


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

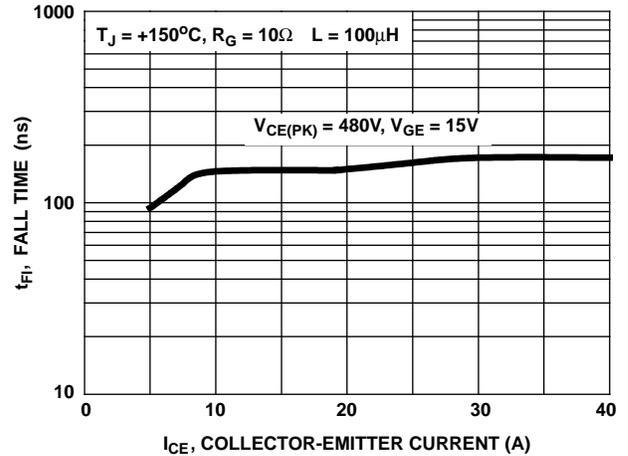


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

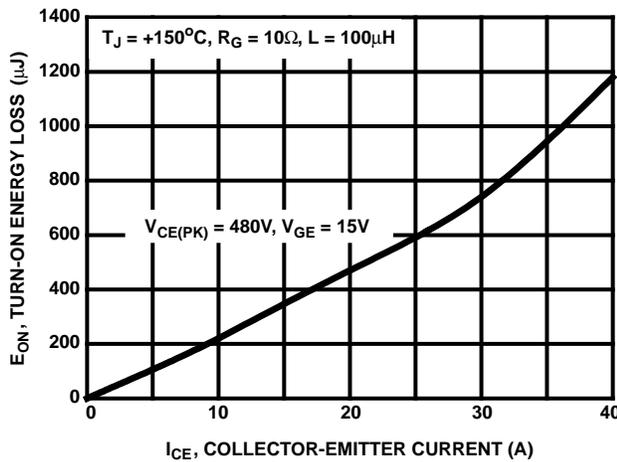


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

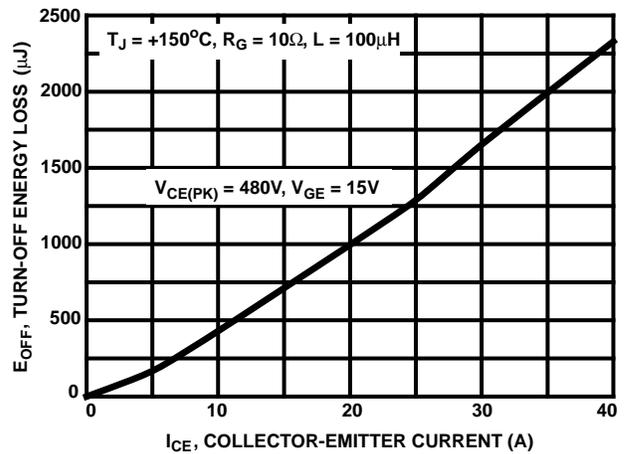


FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

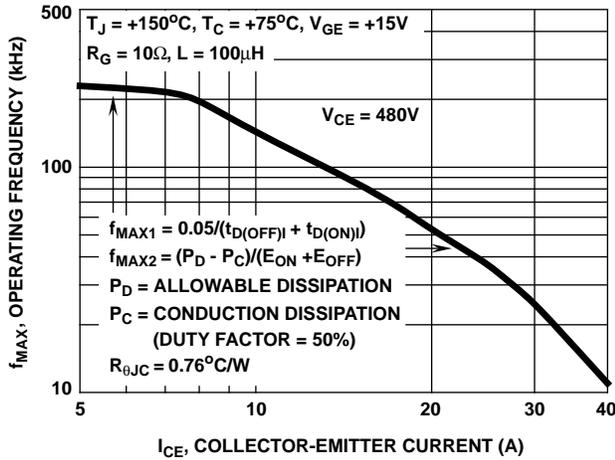


FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

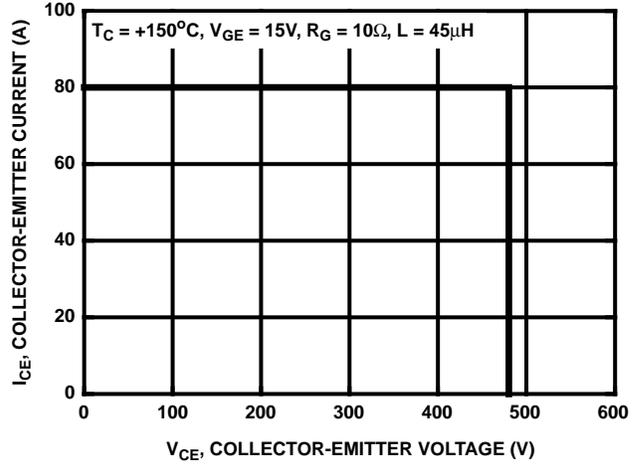


FIGURE 14. SWITCHING SAFE OPERATING AREA

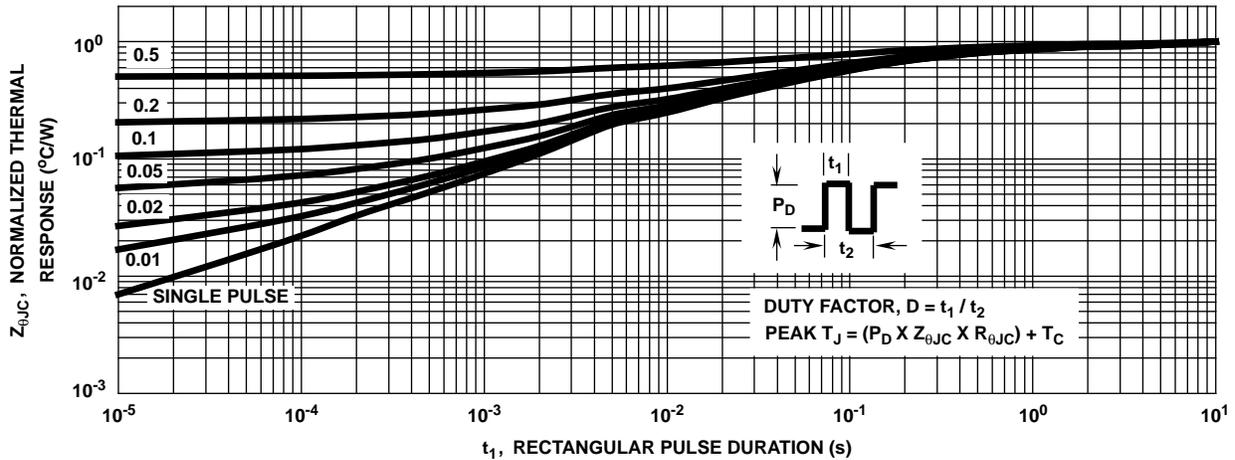


FIGURE 15. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

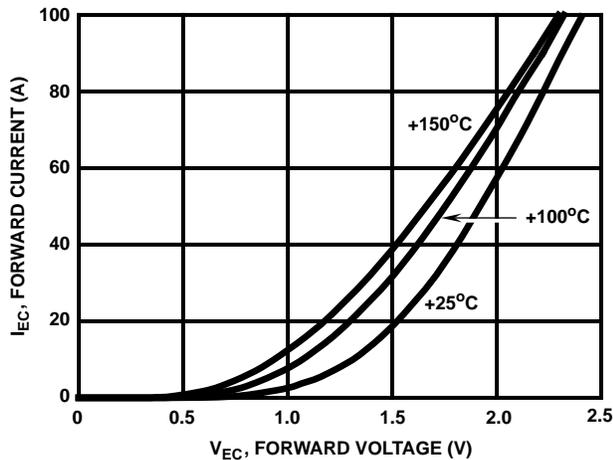


FIGURE 16. DIODE FORWARD CURRENT AS A FUNCTION OF FORWARD VOLTAGE DROP

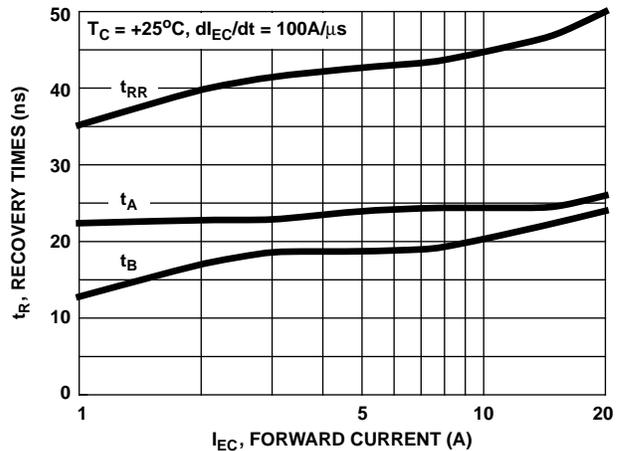


FIGURE 17. RECOVERY TIMES AS A FUNCTION OF FORWARD CURRENT

Test Circuit and Waveforms

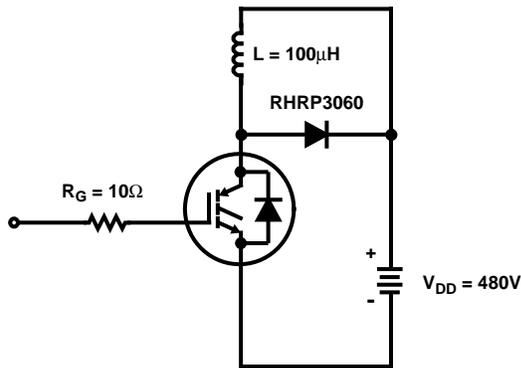


FIGURE 18. INDUCTIVE SWITCHING TEST CIRCUIT

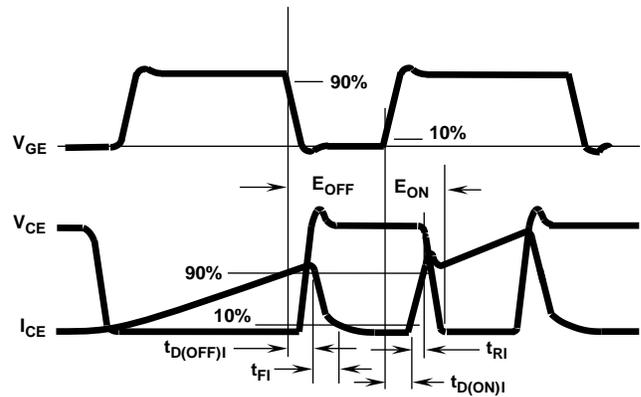


FIGURE 19. SWITCHING TEST WAVEFORMS

Operating Frequency Information

Operating frequency information for a typical device (Figure 13) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05 / (t_{D(OFF)I} + t_{D(ON)I})$. Dead-time (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 19.

Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX} . $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C) / (E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C) / R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D . A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE}) / 2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 19. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss during turn-off. All tail losses are included in the calculation for E_{OFF} ; i.e. the collector current equals zero ($I_{CE} = 0$).

Handling Precautions for IGBT's

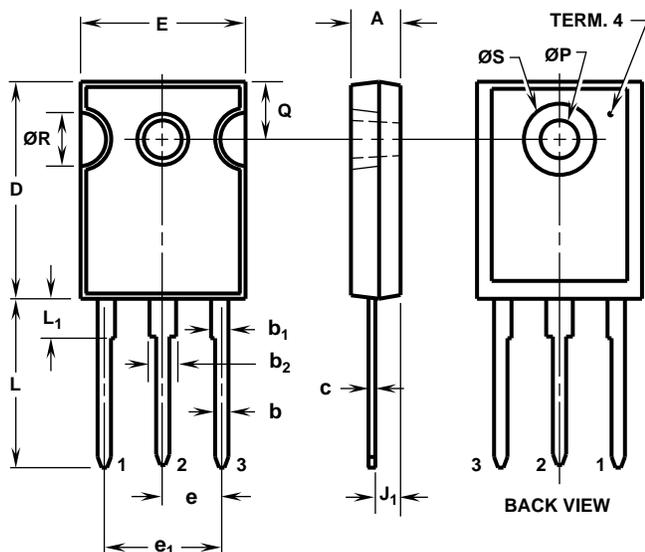
Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and discharge procedures, however, IGBT's are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as †“ECCOSORB LD26” or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM} . Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

† Trademark Emerson and Cumming, Inc.

HGTG20N60B3D

Plastic Packages



TO-247

3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b ₁	0.060	0.070	1.53	1.77	1, 2
b ₂	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e ₁	0.438 BSC		11.12 BSC		4
J ₁	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L ₁	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L₁.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

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