New Jersey Semi-Conductor Products, Inc.

20 STERN AVE.
SPRINGFIELD, NEW JERSEY 07081
U.S.A.

TELEPHONE: (973) 376-2922
(212) 227-6005
FAX: (973) 376-8960

IRF9150
IRF9151

Avalanche Energy Rated P-Channel Power MOSFETs

Features

- -25A, -60V and -100V
- $r_{DS(ON)}$ = 0.150Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

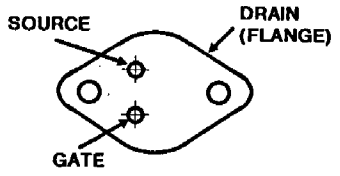
The IRF9150 and IRF9151 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The P-channel IRF9150 is an approximate electrical complement to the N-channel IRF9150.

The IRF types are supplied in the JEDEC TO-204AE metal package.

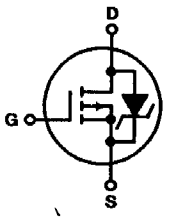
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = 25°C) Unless Otherwise Specified

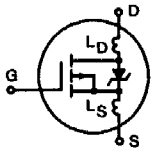
		IRF9150	IRF9151	UNITS
Drain-Source Voltage	V_{DS}	-100	-60	V
Continuous Drain Current				
T_C = 25°C	I_D	-25	-25	A
T_C = 100°C	I_D	-18	-18	A
Pulsed Drain Current	I_{DM}	-100	-100	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation (See Figure 18)	P_D	150	150	W
Linear Derating Factor		1.2	1.2	W/°C
Single Pulse Avalanche Energy Rating (3) (See Figure 14)	E_{as}	1300	1300	mJ
Avalanche Current (Repetitive or Nonrepetitive)	I_{AR}	-25	-25	A
Operating and Storage Junction Temperature Range	TJ, TSTG	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

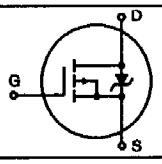
1. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
3. V_{DD} = 25V, Start T_J = +25°C, L = 3.2mhy, R_G = 25Ω, Peak I_L = 19A (See Figures 14 and 15)

Specifications IRF9150, IRF9151

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRF9150	BV_{DSS}	V_{GS} = 0V, I_D = -250µA	-100	-	-	V
IRF9151			-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = -250µA	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = -20V	-	-	-100	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	-250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	-1000	µA
On-State Drain Current (Note 1)	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	-25	-	-	A
Static Drain-Source On-State Resistance (Note 1)	$r_{DS(ON)}$	V_{GS} = -10V, I_D = -10A	-	0.09	0.15	Ω
Forward Transconductance (Note 1)	g_{fs}	V_{DS} = -10V, I_D = -12.5A	4	10	-	S
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz See Figure 10	-	2400	-	pF
Output Capacitance	C_{OSS}		-	850	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	400	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = -50V, I_D = -25A, R_G = 6.8Ω, R_D = 2Ω. See Figures 16 and 17. (MOSFET switching times are essentially independent of operating temperature.)	-	16	24	ns
Rise Time	t_r		-	110	160	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	65	100	ns
Fall Time	t_f		-	46	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = -10V, I_D = -25A, V_{DS} = 0.8 Max Rating. See Figures 11 & 19 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	82	120	nC
Gate-Source Charge	Q_{gs}		-	14	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	42	-	nC
Internal Drain Inductance	L_D	Measured between contact screw on header that is closer to source & gate pins & center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	13	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.83	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.1	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	-25	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-100	A
Diode Forward Voltage (Note 2)	V_{SD}	T_C = +25°C, I_S = 25A, V_{GS} = 0V	-	0.9	1.5	V
Reverse Recovery Time	t_{rr}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/µs	-	150	300	ns
Reverse Recovered Charge	Q_{RR}	T_J = +25°C, I_F = 25A, dI_F/dt = 100A/µs	0.3	0.7	1.5	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%

2. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)

3. V_{DD} = 25V, Start T_J = +25°C, L = 3.2mhy, R_G = 25Ω, Peak I_L = 25A (See Figures 14 and 15)