



**N - CHANNEL ENHANCEMENT MODE
POWER MOS TRANSISTORS**

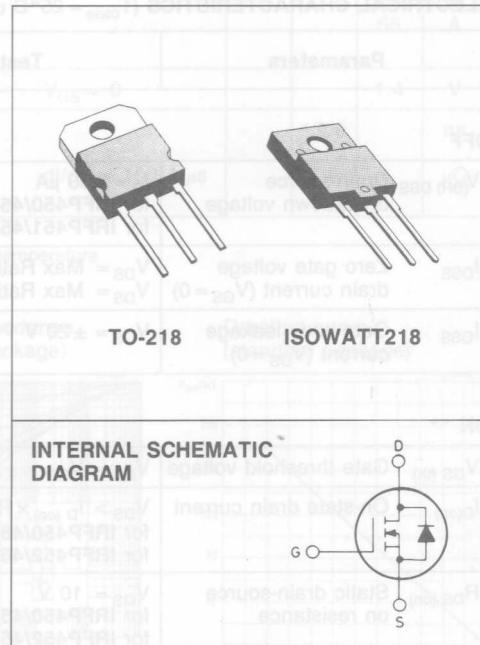
TYPE	V _{DSS}	R _{DS(on)}	I _D ■
IRFP450	500 V	0.4 Ω	14 A
IRFP450FI	500 V	0.4 Ω	9 A
IRFP451	450 V	0.4 Ω	14 A
IRFP451FI	450 V	0.4 Ω	9 A
IRFP452	500 V	0.5 Ω	12 A
IRFP452FI	500 V	0.5 Ω	8 A
IRFP453	450 V	0.5 Ω	12 A
IRFP453FI	450 V	0.5 Ω	8 A

- HIGH VOLTAGE - 450V FOR OFF LINE SMPS
- HIGH CURRENT - 12A FOR UP TO 350W SMPS
- ULTRA FAST SWITCHING - FOR OPERATION AT > 100 KHz
- EASY DRIVE - REDUCES COST AND SIZE

INDUSTRIAL APPLICATIONS:

- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications.



ABSOLUTE MAXIMUM RATINGS

	TO-218	IRFP			
	ISOWATT218	450	451	452	453
		450FI	451FI	452FI	453FI
V _{DS} *	Drain-source voltage (V _{GS} = 0)	500	450	500	450
V _{DGR} *	Drain-gate voltage (R _{GS} = 20 kΩ)	500	450	500	450
V _{GS}	Gate-source voltage			±20	
I _{DM} (•)	Drain current (pulsed)	56	56	48	48
I _{DLM}	Drain inductive current, clamped (L = 100 μH)	56	56	48	48
I _D	Drain current (cont.) at T _c = 25°C	450	451	452	453
I _D	Drain current (cont.) at T _c = 100°C	14	14	12	12
I _D ■	Drain current (cont.) at T _c = 25°C	8.8	8.8	7.9	7.9
I _D ■	Drain current (cont.) at T _c = 100°C	5.6	5.6	5	5
P _{tot} ■	Total dissipation at T _c < 25°C	450FI	451FI	452FI	453FI
	Derating factor	1.80	1.70	0.70	0.55
T _{stg}	Storage temperature	1.44	0.55		
T _j	Max. operating junction temperature			-55 to 150	W/°C
				150	°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature.

■ See note on ISOWATT218 on this datasheet.

THERMAL DATA

TO-218 | ISOWATT218

R_{thj} - case	Thermal resistance junction-case	max	0.69	1.8	$^{\circ}\text{C}/\text{W}$
R_{thc-s}	Thermal resistance case-sink	typ	0.1	$^{\circ}\text{C}/\text{W}$	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	max	30	$^{\circ}\text{C}/\text{W}$	$^{\circ}\text{C}/\text{W}$
T_L	Maximum lead temperature for soldering purpose		300		$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR) DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ for IRFP450/452/450FI/452FI for IRFP451/453/451FI/453FI	$V_{GS} = 0$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$	$T_c = 125^{\circ}\text{C}$			250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$				± 500	na

ON **

$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu\text{A}$	2		4	V
$I_{D(\text{on})}$	On-state drain current	$V_{DS} > I_{D(\text{on})} \times R_{DS(\text{on}) \text{ max}}$ for IRFP450/451/450FI/451FI for IRFP452/453/452FI/453FI	$V_{GS} = 10 \text{ V}$	14			A
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$ for IRFP450/451/450FI/451FI for IRFP452/453/452FI/453FI	$I_D = 7.9 \text{ A}$			0.4 0.5	Ω Ω

DYNAMIC

g_{fs}^{**}	Forward transconductance	$V_{DS} > I_{D(\text{on})} \times R_{DS(\text{on}) \text{ max}}$ $I_D = 7.9 \text{ A}$		9.3			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$	$f = 1 \text{ MHz}$			3000 600 200	pF pF pF

SWITCHING

$t_d(\text{on})$	Turn-on time	$V_{DD} = 210 \text{ V}$	$I_D = 7.0 \text{ A}$			35	ns
t_r	Rise time	$R_i = 4.7 \Omega$				50	ns
$t_d(\text{off})$	Turn-off delay time		(see test circuit)			150	ns
t_f	Fall time					70	ns
Q_g	Total Gate Charge	$V_{GS} = 10 \text{ V}$	$I_D = 13 \text{ A}$			120	nC
		$V_{DS} = \text{Max Rating} \times 0.8$	(see test circuit)				

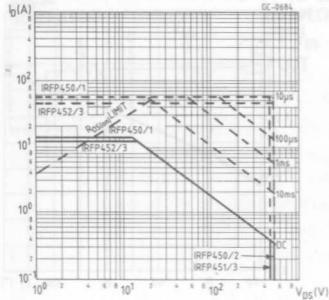
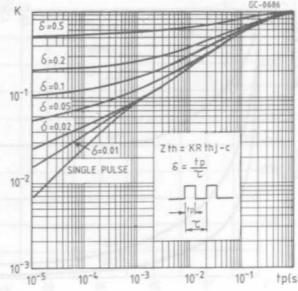
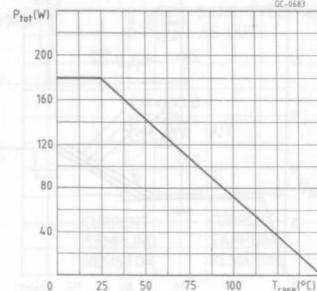
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD}	Source-drain current			14	A
$I_{SDM} (\text{puls})$	Source-drain current (pulsed)			56	A
V_{SD}	Forward on voltage	$I_{SD} = 14 \text{ A}$	$V_{GS} = 0$	1.4	V
t_{rr}	Reverse recovery time	$T_j = 150^\circ\text{C}$		1300	ns
Q_{rr}	Reverse recovered charge	$I_{SD} = 14 \text{ A}$	$dI/dt = 100 \text{ A}/\mu\text{s}$	7.4	μC

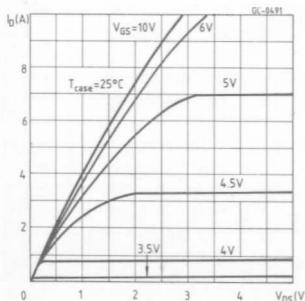
** Pulsed: Pulse duration $\leq 300 \mu\text{s}$, duty cycle $\leq 1.5\%$

(*) Repetitive Rating: Pulse width limited by max junction temperature

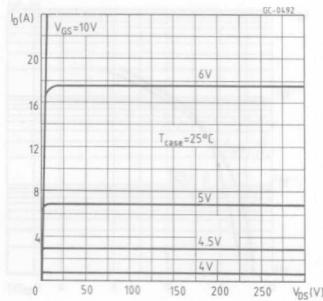
■ See note on ISOWATT218 in this datasheet.

Safe operating areas
(standard package)Thermal impedance
(standard package)Derating curve
(standard package)

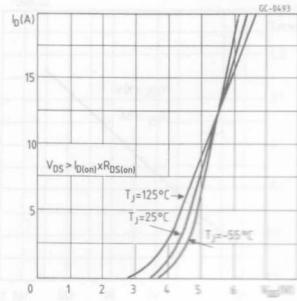
Output characteristics



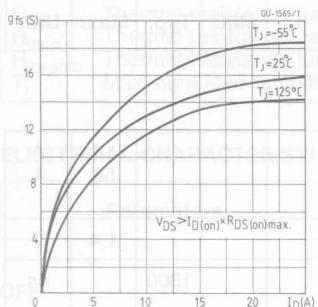
Output characteristics



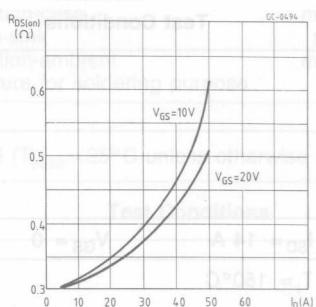
Transfer characteristics



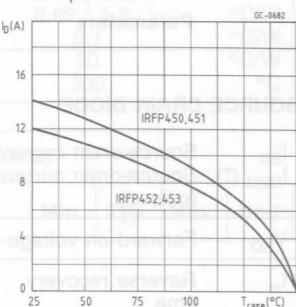
Transconductance



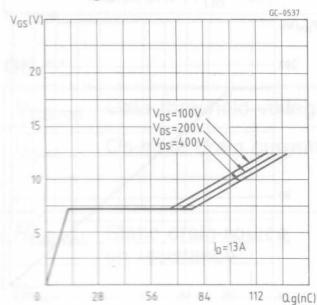
Static drain-source on resistance



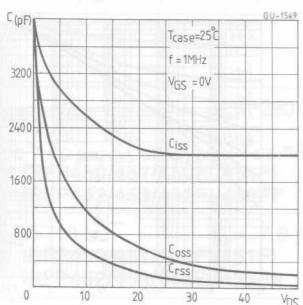
Maximum drain current vs temperature



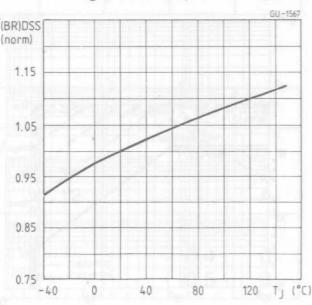
Gate charge vs gate-source voltage



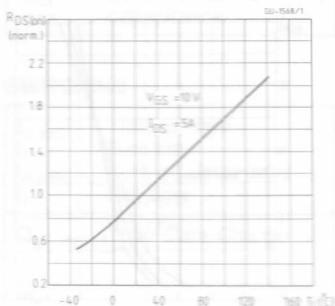
Capacitance variation



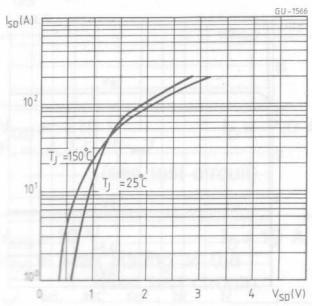
Normalized breakdown voltage vs temperature



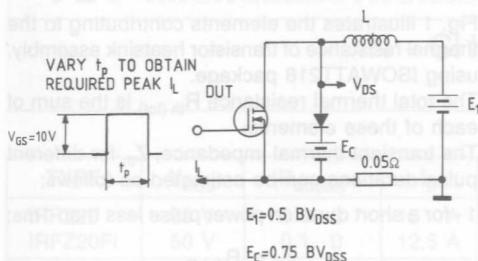
Normalized on resistance vs temperature



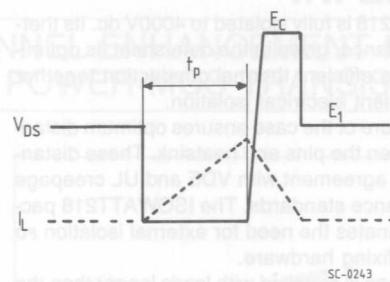
Source-drain diode forward characteristics



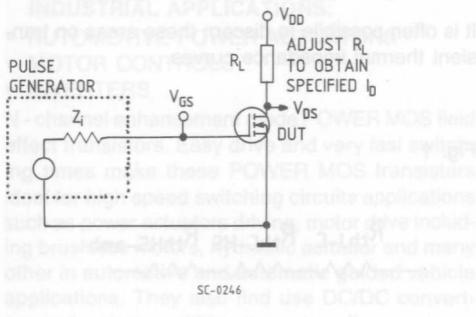
Clamped inductive test circuit



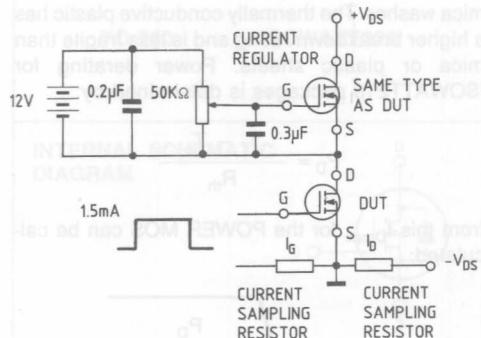
Clamped inductive waveforms

N-CHANNEL POWER MOS TRANSISTORS
to switch inductors to obtain power gain and EASY DRIVING

Switching times test circuit



Gate charge test circuit



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)
V_{DSS}	Drain-gate voltage ($I_{DS} = 20 \text{ mA}$)
V_{GS}	Gate-source voltage
I_{DS} (A)	Drain current (clamped)
I_{DS} (mA)	Drain current, clamped to -1000 mA

Drain current (I_{DS}) at $T_c = 25^\circ\text{C}$	1000 mA
Drain current (I_{DS}) at $T_c = 150^\circ\text{C}$	100 mA
Drain current (I_{DS}) at $T_c = -55^\circ\text{C}$	1000 mA
Drain current (I_{DS}) at $T_c = 100^\circ\text{C}$	100 mA
Total dissipation at $T_c < 150^\circ\text{C}$	100 W
Operating voltage	1000 V
Storage temperature	150°C
Storage temperature (option)	200°C
Drain-to-source voltage range	-1000 to 1000 V
Drain-to-gate voltage range	-1000 to 1000 V
Drain-to-source current range	-1000 to 1000 mA
Drain-to-gate current range	-1000 to 1000 mA

ISOWATT218 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT218 is fully isolated to 4000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.

The structure of the case ensures optimum distances between the pins and heatsink. These distances are in agreement with VDE and UL creepage and clearance standards. The ISOWATT218 package eliminates the need for external isolation so reducing fixing hardware.

The package is supplied with leads longer than the standard TO-218 to allow easy mounting on PCBs. Accurate moulding techniques used in manufacture assures consistent heat spreader-to-heatsink capacitance.

ISOWATT218 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT218 packages is determined by:

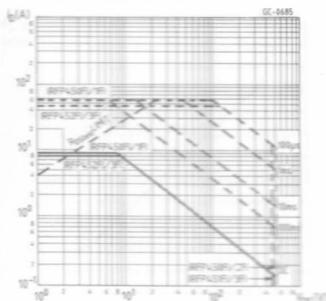
$$P_D = \frac{T_J - T_C}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

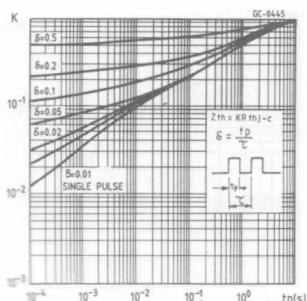
$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)} \text{ (at } 150^\circ\text{C)}}}$$

ISOWATT DATA

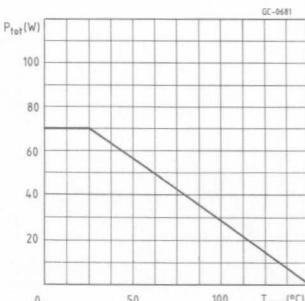
Safe operating areas



Thermal impedance



Derating curve



THERMAL IMPEDANCE OF ISOWATT218 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT218 package.

The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.

The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ-C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

$$Z_{th} = R_{thJ-C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ-C} + R_{thC-HS} + R_{thHS-amb}$$

It is often possible to discern these areas on transient thermal impedance curves.

Fig. 1

