

# IRLMS1902

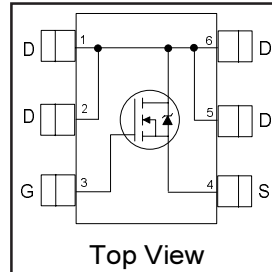
HEXFET® Power MOSFET

- Generation V Technology
- Micro6 Package Style
- Ultra Low Rds(on)
- N-Channel MOSFET

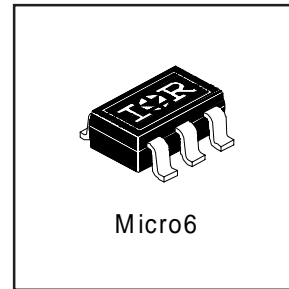
## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The Micro6 package with its customized leadframe produces a HEXFET power MOSFET with Rds(on) 60% less than a similar size SOT-23. This package is ideal for applications where printed circuit board space is at a premium. It's unique thermal design and R<sub>DS(on)</sub> reduction enables a current-handling increase of nearly 300% compared to the SOT-23.



$V_{DSS} = 20V$
$R_{DS(on)} = 0.10\Omega$



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	3.2	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	2.6	
$I_{DM}$	Pulsed Drain Current ①	18	
$P_D @ T_A = 25^\circ C$	Power Dissipation	1.7	W
	Linear Derating Factor	13	mW/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 12$	V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	V/ns
$T_J, T_{STG}$	Junction and Storage Temperature Range	-55 to +150	°C

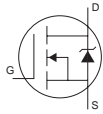
## Thermal Resistance Ratings

	Parameter	Min.	Typ.	Max	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	—	—	75	°C/W

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.032	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.10	$\Omega$	$V_{GS} = 4.5V, I_D = 2.2A$ ③
		—	—	0.17		$V_{GS} = 2.7V, I_D = 1.1A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	0.70	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	3.2	—	—	S	$V_{DS} = 10V, I_D = 1.1A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	$\mu A$	$V_{DS} = 16V, V_{GS} = 0V$
		—	—	25		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 12V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -12V$
$Q_g$	Total Gate Charge	—	4.7	7.0	nC	$I_D = 2.2A$
$Q_{gs}$	Gate-to-Source Charge	—	0.97	1.5		$V_{DS} = 16V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	1.8	2.6		$V_{GS} = 4.5V$ , See Fig. 6 and 9 ③
$t_{d(on)}$	Turn-On Delay Time	—	7.0	—		$V_{DD} = 10V$
$t_r$	Rise Time	—	11	—	ns	$I_D = 2.2A$
$t_{d(off)}$	Turn-Off Delay Time	—	12	—		$R_G = 6.0\Omega$
$t_f$	Fall Time	—	4.0	—		$R_D = 4.4\Omega$ , See Fig. 10 ③
$C_{iss}$	Input Capacitance	—	300	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	120	—		$V_{DS} = 15V$
$C_{rss}$	Reverse Transfer Capacitance	—	50	—		$f = 1.0\text{MHz}$ , See Fig. 5

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	1.7	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	18		
$V_{SD}$	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 2.2A, V_{GS} = 0V$ ②
$t_{rr}$	Reverse Recovery Time	—	40	60	ns	$T_J = 25^\circ\text{C}, I_F = 2.2A$
$Q_{rr}$	Reverse Recovery Charge	—	37	55	nC	$di/dt = 100A/\mu s$ ②

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ②  $I_{SD} \leq 2.2A, di/dt \leq 110A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ③ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ④ Surface mounted on FR-4 board,  $t \leq 5\text{sec}$ .

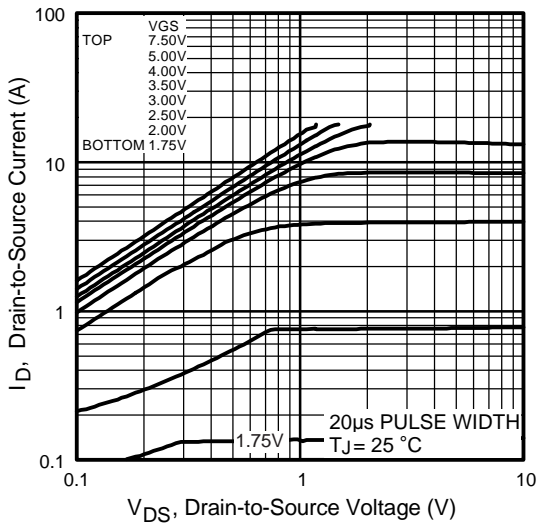


Fig 1. Typical Output Characteristics

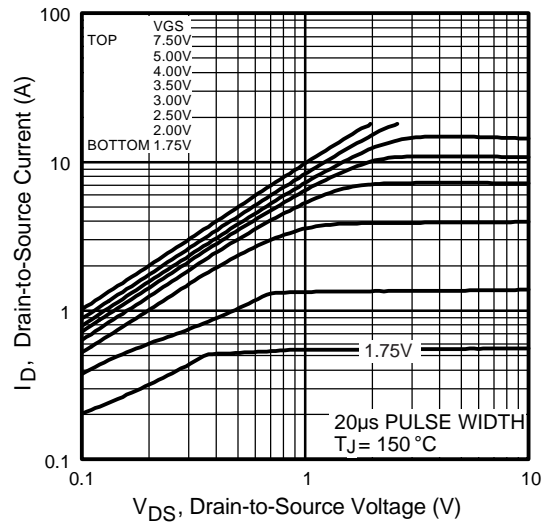


Fig 2. Typical Output Characteristics

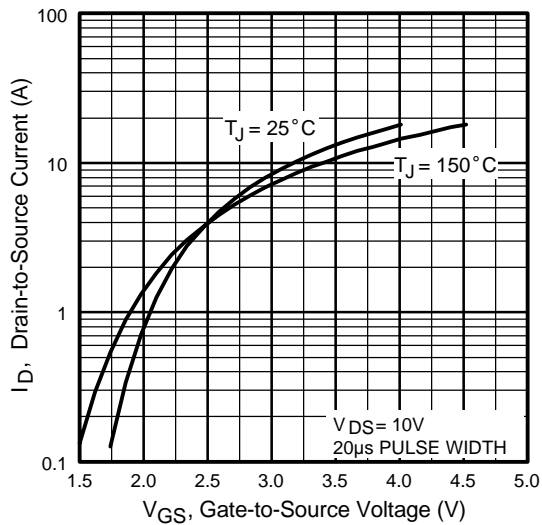


Fig 3. Typical Transfer Characteristics

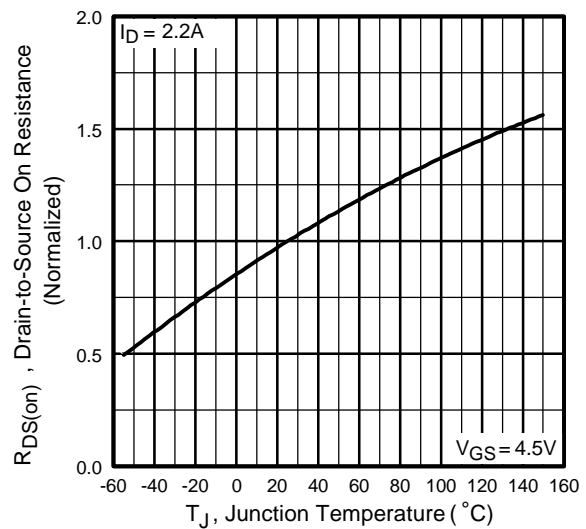
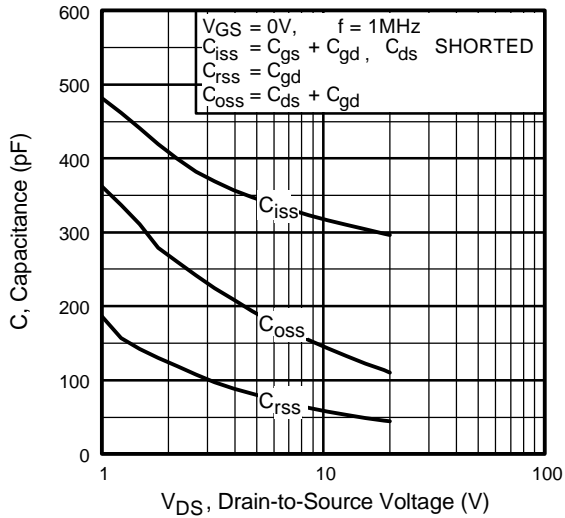
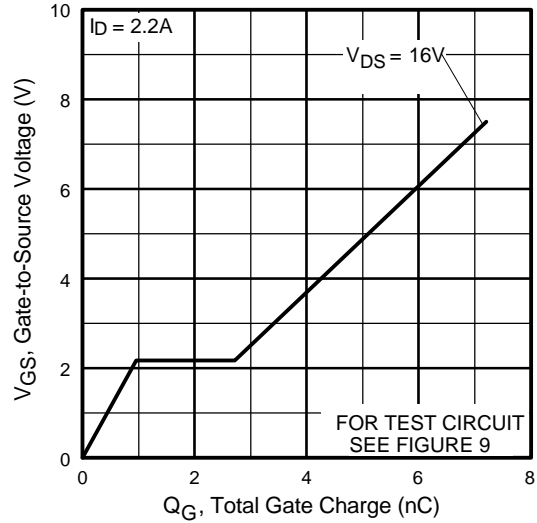


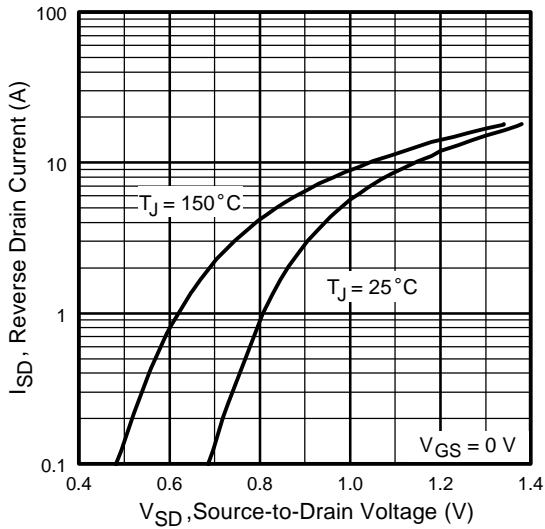
Fig 4. Normalized On-Resistance Vs. Temperature



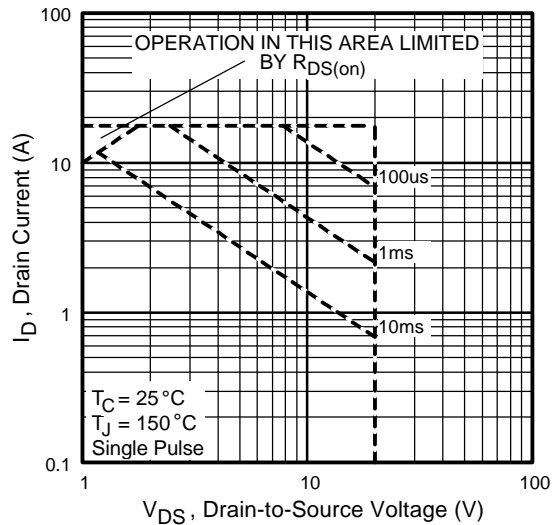
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

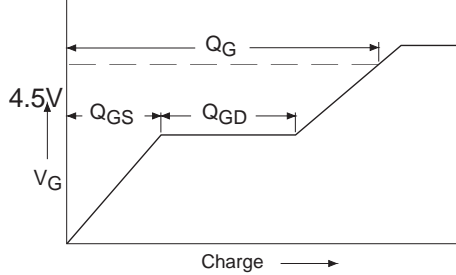


Fig 9a. Basic Gate Charge Waveform

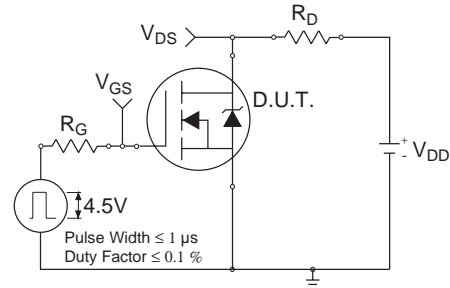


Fig 10a. Switching Time Test Circuit

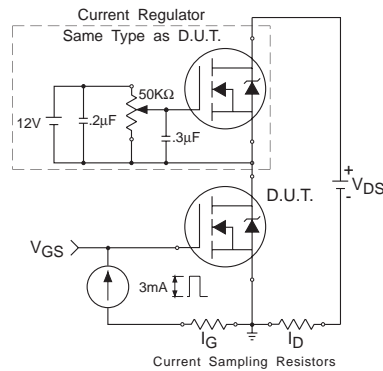


Fig 9b. Gate Charge Test Circuit

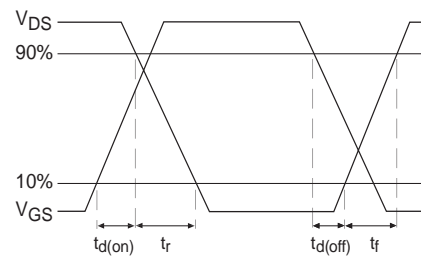


Fig 10b. Switching Time Waveforms

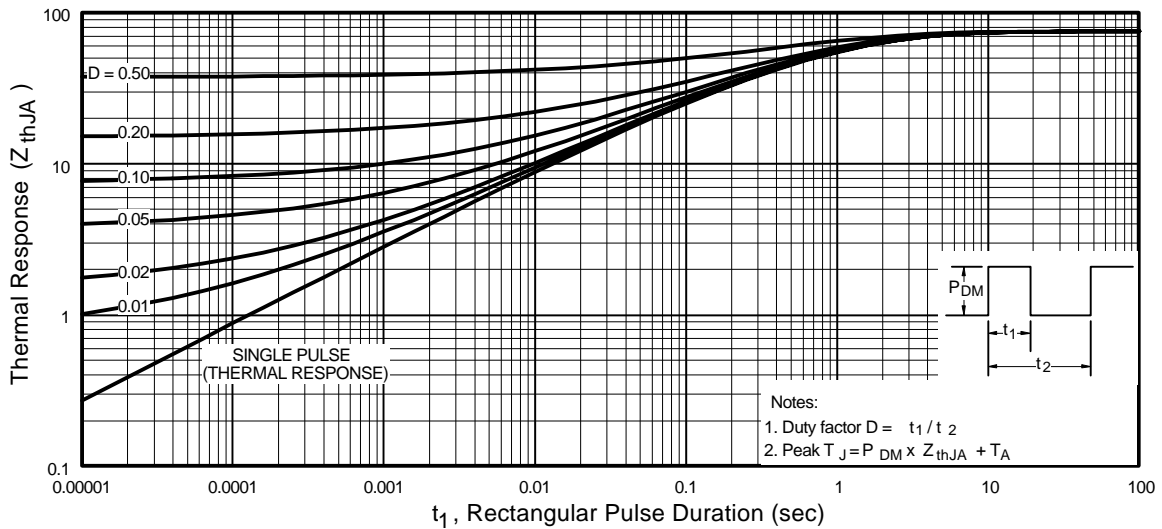
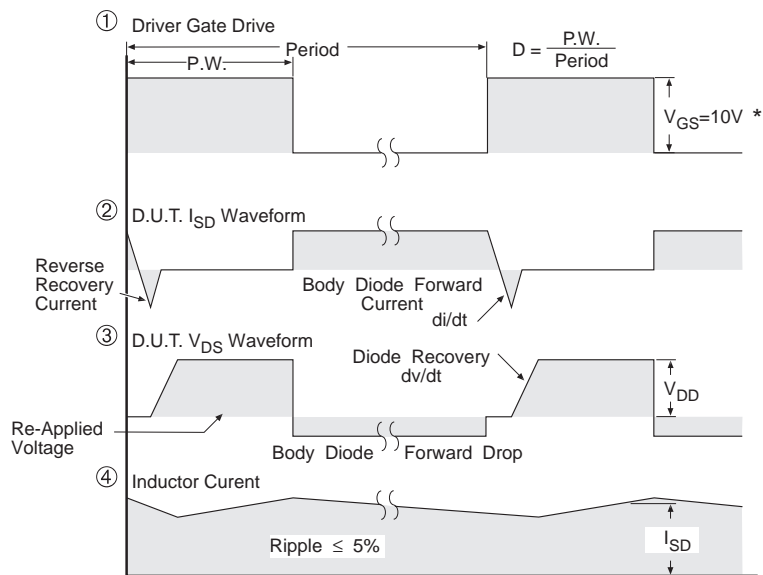
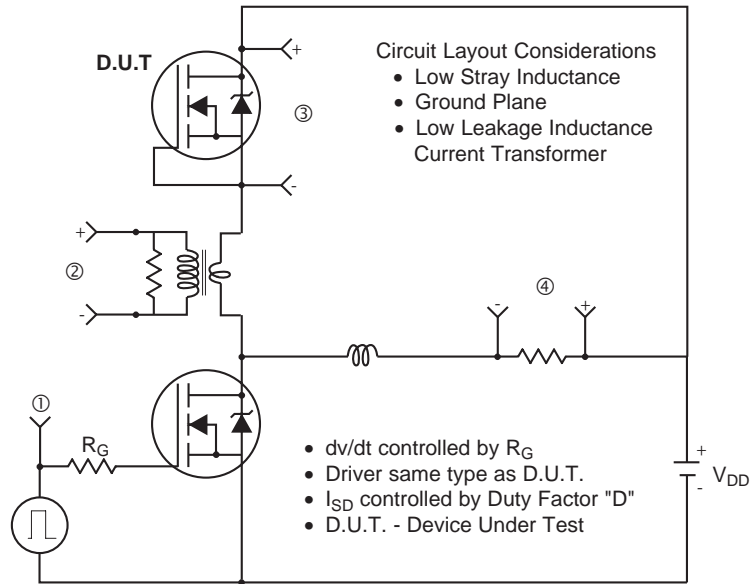


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

**Peak Diode Recovery dv/dt Test Circuit**

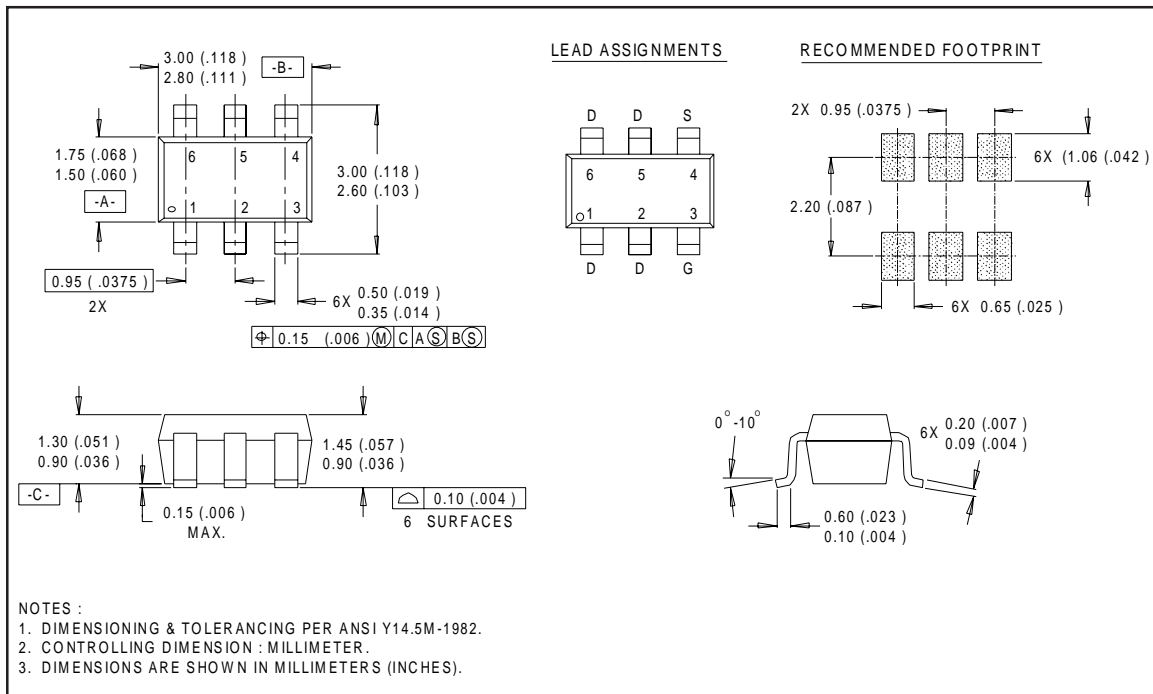


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 12.** For N-Channel HEXFETS

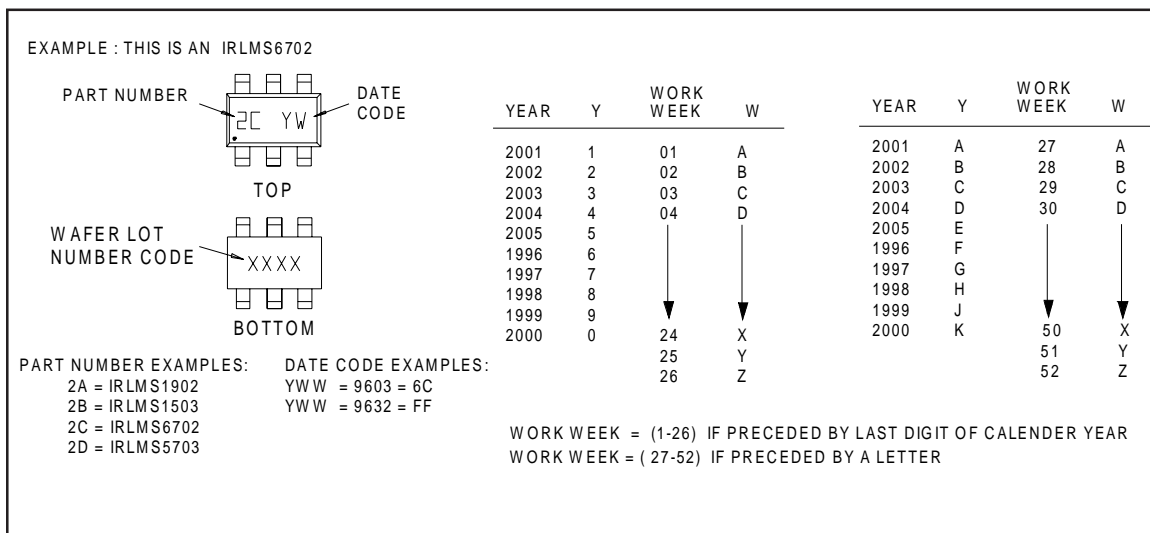
## Package Outline

### Micro6 Outline



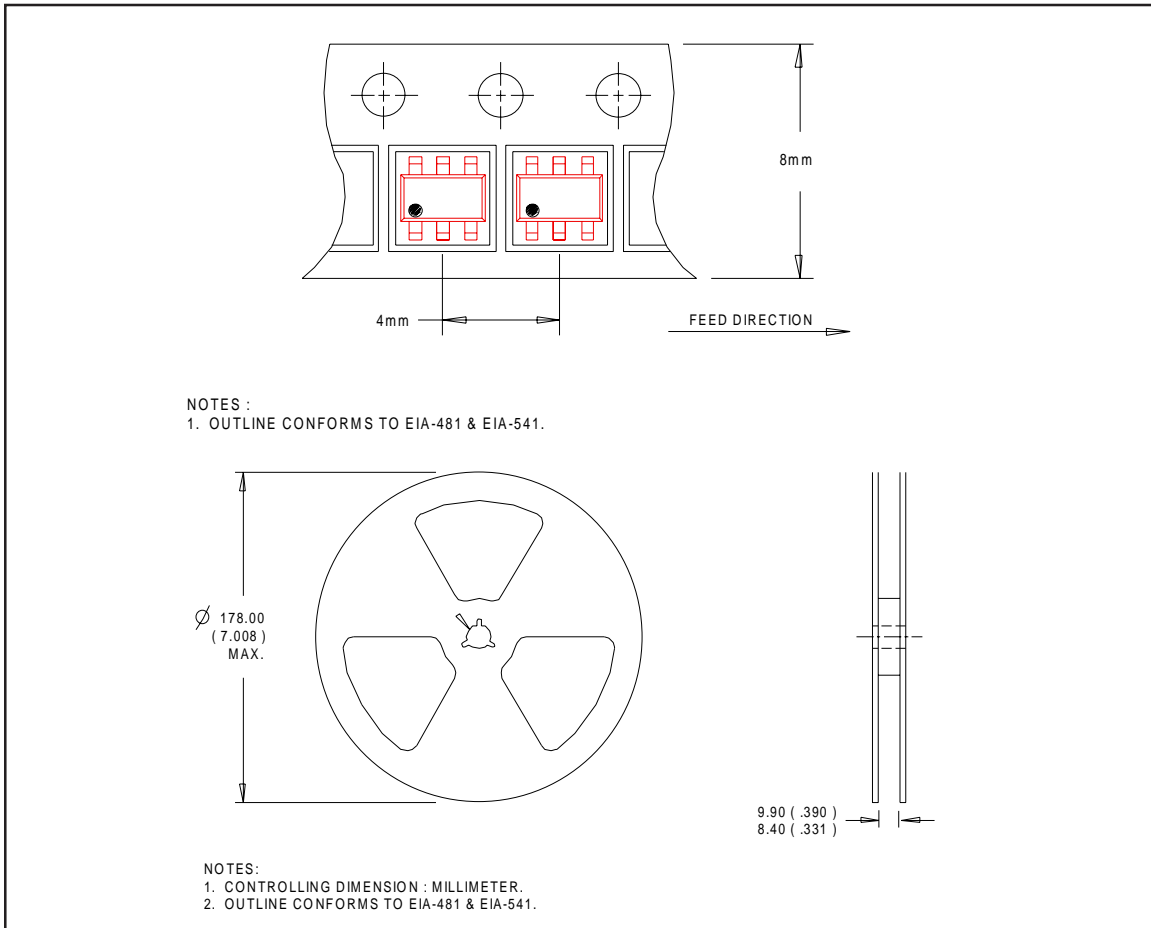
## Part Marking Information

### Micro6



## Tape & Reel Information

### Micro6



International  
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