

December 2011

# **KSC2331 NPN Epitaxial Silicon Transistor**

### **Features**

- · Low Frequency Amplifier & Medium Speed Switching
- Complement to KSA931
- High Collector-Base Voltage : V<sub>CBO</sub>=80V
- Collector Current : I<sub>C</sub>=700mA
   Collector Dissipation : P<sub>C</sub>=1W



1. Emitter 2. Collector 3. Base

## **Absolute Maximum Ratings** $T_a = 25$ °C unless otherwise noted

Symbol	Parameter	Value	Units
V <sub>CBO</sub>	Collector-Base Voltage	80	V
$V_{CEO}$	Collector-Emitter Voltage	60	V
$V_{EBO}$	Emitter-Base Voltage	8	V
I <sub>C</sub>	Collector Current	700	mA
P <sub>C</sub>	Collector Power Dissipation	1	W
T <sub>J</sub>	Junction Temperature	150	°C
T <sub>STG</sub>	Storage Temperature	-55 to 150	°C

## **Electrical Characteristics** $T_a = 25$ °C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
BV <sub>CBO</sub>	Collector-Base Breakdown Voltage	I <sub>C</sub> =100μA, I <sub>E</sub> =0	80			V
BV <sub>CEO</sub>	Collector-Emitter Breakdown Voltage	I <sub>C</sub> =10mA, I <sub>B</sub> =0	60			V
BV <sub>EBO</sub>	Emitter-Base Breakdown Voltage	I <sub>E</sub> =10μA, I <sub>C</sub> =0	8			V
I <sub>CBO</sub>	Collector Cut-off Current	$V_{CB}$ =60V, $I_E$ =0			0.1	μΑ
I <sub>EBO</sub>	Emitter Cut-off Current	$V_{EB}$ =5V, $I_{C}$ =0			0.1	μΑ
h <sub>FE</sub>	DC Current Gain	$V_{CE}$ =2V, $I_{C}$ =50mA	40		240	
V <sub>CE</sub> (sat)	Collector-Emitter Saturation Voltage	I <sub>C</sub> =500mA, I <sub>B</sub> =50mA		0.2	0.7	V
V <sub>BE</sub> (sat)	Base-Emitter Saturation Voltage	I <sub>C</sub> =500mA, I <sub>B</sub> =50mA		0.86	1.20	V

## **h**<sub>FE</sub> Classification

Classification	R	0	Y
h <sub>FE</sub>	40 ~ 80	70 ~ 140	120 ~ 240

# **Typical Performance Characteristics**

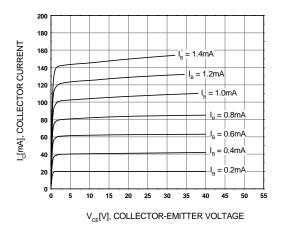


Figure 1. Static Characteristic

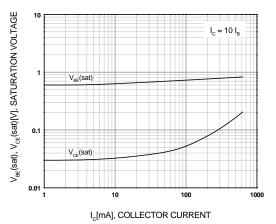


Figure 3. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

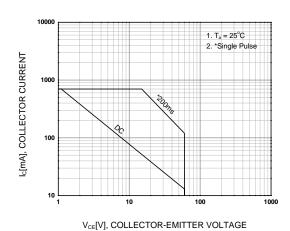


Figure 5. Safe Operating Area

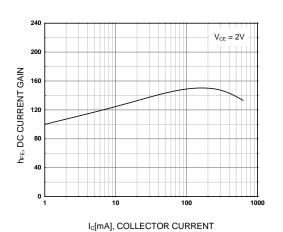


Figure 2. DC current Gain

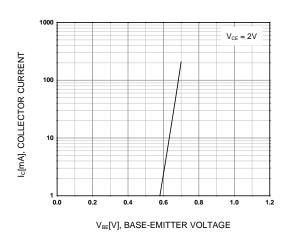


Figure 4. Base-Emitter On Voltage

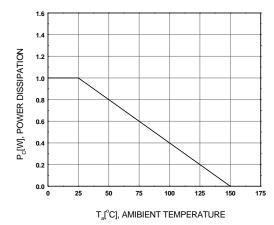


Figure 6. Power Derating





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