

New Jersey Semi-Conductor Products, Inc.

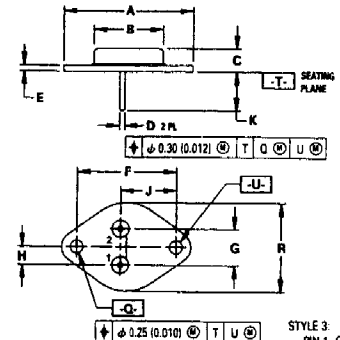
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MTM24N50

TMOS Power Field Effect Transistors N-Channel Enhancement-Mode Silicon Gate

Symbol	Test Conditions	Maximum Ratings	
V_{DS}	$T_J = 25^\circ\text{C}$ to 150°C	500	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1\text{ M}\Omega$	500	V
V_{GS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	24	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	96	A
P_D	$T_C = 25^\circ\text{C}$	300	W
T_J		$-55 \dots +150$	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		$-55 \dots +150$	$^\circ\text{C}$
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		300	$^\circ\text{C}$



DIM	MIN	MAX	MIN	MAX
A	38.35	39.37	1.510	1.550
B	19.31	21.09	0.760	0.830
C	5.35	8.25	0.210	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

TO-204AE

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 0.25\text{ mA}$)	$V_{(BR)DSS}$	500	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = \text{Rated } V_{DSS}$, $V_{GS} = 0$) ($V_{DS} = 0.8 \text{ Rated } V_{DSS}$, $V_{GS} = 0$, $T_J = 125^\circ\text{C}$)	I_{DSS}	—	0.25 1.00	mAdc
Gate-Body Leakage Current, Forward ($V_{GSF} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 0.25\text{ mA}$)	$V_{GS(th)}$	2.0	4.0	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 12\text{ A}$)	$r_{DS(on)}$	—	0.25	Ohm
Forward Transconductance ($V_{DS} = 10\text{ V}$, $I_D = 12\text{ A}$)	g_{FS}	11	16	mhos

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Quality Semi-Conductors