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MTP25N05E

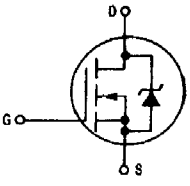
TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

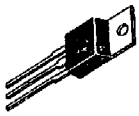
TMOS POWER FETs
25 AMPERES
$r_{DS(on)}$ = 0.07 OHM
50 VOLTS

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

TMOS™





TO-220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	50	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	25 80	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.25 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	50	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μA
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA, T_J = 100°C)		$V_{GS(th)}$	2 1.5	4 3.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 16 Adc)		$r_{DS(on)}$	—	0.07	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 25 Adc) (I_D = 12.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	2 1	Vdc
Forward Transconductance (V_{DS} = 1.75 V, I_D = 16 A)		g_{FS}	9	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS					
Unclamped Drain-to-Source Avalanche Energy See Figures 14 and 15 (I_D = 80 A, V_{DD} = 25 V, T_C = 25°C, Single Pulse, Non-repetitive) (I_D = 25 A, V_{DD} = 25 V, T_C = 25°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%) (I_D = 10 A, V_{DD} = 25 V, T_C = 100°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)		W_{DSR}	— — —	90 200 90	mJ
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 16	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	800	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 16 A, R_{gen} = 15 ohms) See Figure 9	$t_{d(on)}$	—	25	ns
Rise Time		t_r	—	35	
Turn-Off Delay Time		$t_{d(off)}$	—	45	
Fall Time		t_f	—	35	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	26 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	14 (Typ)	—	
Gate-Drain Charge		Q_{gd}	12 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 25 A, V_{GS} = 0)	V_{SD}	1.3 (Typ)	1.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	160 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.