New Jersey Semi-Conductor Products, Inc.

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MTM2N85
MTM2N90
MTP2N85
MTP2N90

Designer's Data Sheet

Power Field Effect Transistor

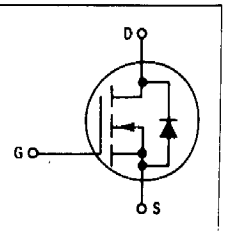
N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS

TMOS POWER FETs
2 AMPERES
$r_{DS(on)}$ = 8 OHMS
850 and 900 VOLTS

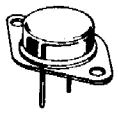


MAXIMUM RATINGS

Rating	Symbol	MTM2N85 / MTP2N85	MTM2N90 / MTP2N90	Unit
Drain-Source Voltage	V_{DSS}	850	900	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	850	900	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	2 7		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta JA}$	30	
	TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		T_L	275	°C



MTM2N85
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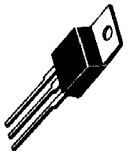
TO-204AA



MTP2N85
MTP2N90

TO-220AB

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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTM/MTP2N85 MTM/MTP2N90		$V_{(BR)DSS}$	850 900	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1 Adc)		$r_{DS(on)}$	—	8	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 2 Adc) (I_D = 1 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	20 16	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 1 A)		g_{FS}	0.5	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	80	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Turn-On Delay Time	(V_{DD} = 125 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	33 (Typ)	40	nC
Gate-Source Charge		Q_{gs}	20 (Typ)	—	
Gate-Drain Charge		Q_{gd}	13 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1 (Typ)	1.4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	420 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE (TO-204)

Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)	L_s	12.5 (Typ)	—	

INTERNAL PACKAGE INDUCTANCE (TO-220)

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

Quality Semi-Conductors