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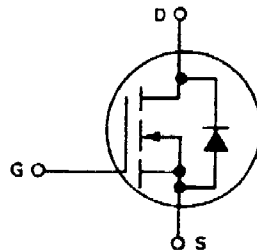
**MTP4N08, MTP5N05
 MTP4N10, MTP5N06**

Designer's Data Sheet

**N-CHANNEL ENHANCEMENT MODE SILICON GATE
 TMOS POWER FIELD EFFECT TRANSISTOR**

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

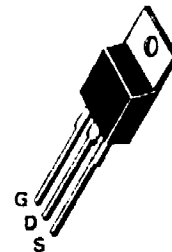
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



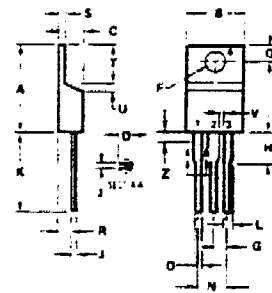
**4.0 and 5.0 AMPERE
 N-CHANNEL TMOS
 POWER FET**

$r_{DS(on)} = 0.8 \text{ OHM}$
 80 and 100 VOLTS

$r_{DS(on)} = 0.6 \text{ OHM}$
 50 and 60 VOLTS



**MTP4N08
 MTP4N10
 MTP5N05
 MTP5N06**



STYLE S
 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	15.11	15.75	0.595	0.620
B	3.81	4.25	0.150	0.168
C	4.06	4.82	0.160	0.190
D	0.84	0.88	0.033	0.035
E	3.81	3.75	0.150	0.147
F	2.64	2.87	0.104	0.113
G	2.79	3.30	0.110	0.130
H	0.50	0.56	0.019	0.022
K	12.70	16.27	0.500	0.643
L	1.14	1.30	0.045	0.051
M	0.25	0.30	0.010	0.012
N	2.54	3.05	0.100	0.120
P	2.04	2.79	0.080	0.110
S	1.14	1.30	0.045	0.051
T	5.97	6.48	0.235	0.254
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-
Z	-	2.00	-	0.078

MAXIMUM RATINGS

Rating	Symbol	MTP				Unit
		5N05	5N06	4N08	4N10	
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Drain Current Continuous	I_D	5.0		4.0		Adc
Pulsed	I_{DM}	10		9.0		
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	50				Watts
		0.4				W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150				$^\circ\text{C}$

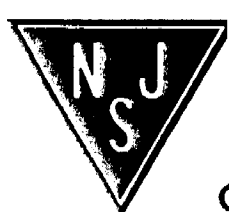
THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ\text{C}$

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

TO-220AB



ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 5.0 \text{ mA}$)	$V_{(BR)DSS}$	50 60 80 100	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 0.85 \text{ Rated } V_{DSS}, V_{GS} = 0$) ($T_J = 100^\circ\text{C}$)	I_{DSS}	—	0.25 2.5	mAdc
Gate-Body Leakage Current ($V_{GS} = 20 \text{ Vdc}, V_{DS} = 0$)	I_{GSS}	—	500	nAdc

ON CHARACTERISTICS*				
Gate Threshold Voltage ($I_D = 1.0 \text{ mA}, V_{DS} = V_{GS}$) ($T_J = 100^\circ\text{C}$)	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10 \text{ Vdc}, I_D = 2.5 \text{ Adc}$) ($V_{GS} = 10 \text{ Vdc}, I_D = 2.0 \text{ Adc}$)	$r_{DS(on)}$	—	0.6 0.8	Ohms
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 5.0 \text{ Adc}$) ($I_D = 2.5 \text{ Adc}, T_J = 100^\circ\text{C}$) ($I_D = 4.0 \text{ Adc}$) ($I_D = 2.0 \text{ Adc}, T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	—	3.75 3.0 4.8 3.2	Vdc
Forward Transconductance ($V_{DS} = 15 \text{ V}, I_D = 2.5 \text{ A}$) ($V_{DS} = 15 \text{ V}, I_D = 2.0 \text{ A}$)	g_{fs}	0.75 0.75	—	mhos

DYNAMIC CHARACTERISTICS				
Input Capacitance ($V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$)	C_{iss}	—	300	pF
Output Capacitance ($V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$)	C_{oss}	—	250	pF
Reverse Transfer Capacitance ($V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$)	C_{rss}	—	60	pF

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)					
Turn-On Delay Time	($V_{DS} = 25 \text{ V}, I_D = 0.5 \text{ Rated } I_D,$ $R_{gen} = 50 \text{ ohms},$ See Figures 1 and 2)	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	80	
Turn-Off Delay Time		$t_{d(off)}$	—	30	
Fall Time		t_f	—	30	

SOURCE DRAIN DIODE CHARACTERISTICS*				
Characteristic	Symbol	Typ	Unit	
Forward On-Voltage ($I_S = \text{Rated } I_D,$ $V_{GS} = 0.$)	V_{SD}	2.5	Vdc	
Forward Turn-On Time	t_{on}	150	ns	
Reverse Recovery Time	t_{rr}	250	ns	

*Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

FIGURE 1 — SWITCHING TEST CIRCUIT

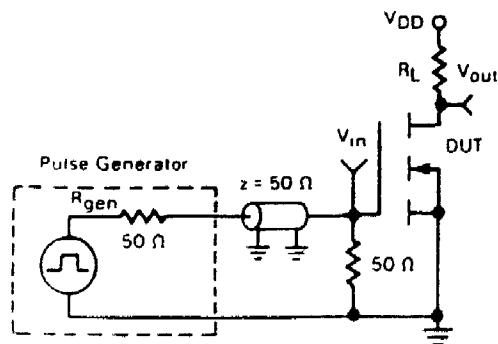


FIGURE 2 — SWITCHING WAVEFORMS

