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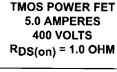
## TMOS E-FET ™ High Energy Power FET

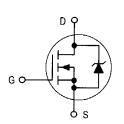
N-Channel Enhancement-Mode Silicon Gate

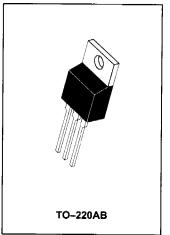
This advanced high voltage TMOS E-FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source-to-Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode









#### MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	400	Vdc
Drain-Gate Voltage (RGS = 1.0 M $\Omega$ )	VDGR	400	Vdc
Gate-Source Voltage — Continuous — Non-repetitive	V <sub>GS</sub> V <sub>GSM</sub>	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I <sub>D</sub>	5.0 12	Adc
Total Power Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	PD	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C

#### UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS (TJ < 150°C)

Single Pulse Drain-to-Source Avalanche Energy — T <sub>J</sub> = 25°C	W <sub>DSR</sub> (1)	290	mJ
— T <sub>J</sub> = 100°C		46	
Repetitive Pulse Drain-to-Source Avalanche Energy	W <sub>DSR</sub> (2)	7.4	

#### THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	R <sub>0</sub> JC R <sub>0</sub> JA	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

**Quality Semi-Conductors** 

#### MTP5N40E

### **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

Cha	racteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS	and the second s					
Drain-to-Source Breakdown Voltag (V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μAdc)	ge	V(BR)DSS	400	_	_	Vdc
Zero Gate Voltage Drain Current (VDS = 400 V, VGS = 0) (VDS = 320 V, VGS = 0, TJ = 125	5°C)	IDSS	_	<u>-</u>	0.25 1.0	mAdc
Gate-Body Leakage Current, Forw	Gate-Body Leakage Current, Forward (V <sub>GSF</sub> = 20 Vdc, V <sub>DS</sub> = 0)			_	100	nAdc
Gate-Body Leakage Current, Reve	erse (V <sub>GSR</sub> = 20 Vdc, V <sub>DS</sub> = 0)	IGSSR	_	_	100	nAdc
ON CHARACTERISTICS*						_
Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) (T <sub>J</sub> = 125°C)		VGS(th)	2.0 1.5	_	4.0 3.5	Vdc
Static Drain-Source On-Resistance	e (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 2.5 Adc)	R <sub>DS(on)</sub>	_	0.8	1.0	Ohm
Drain-Source On-Voltage (VGS = (ID = 5.0 A) (ID = 2.5 A, TJ = 100°C)	10 Vdc)	V <sub>DS(on)</sub>	_	_	6.2 5.0	Vdc
Forward Transconductance (VDS =	15 Vdc, I <sub>D</sub> = 2.5 Adc)	9FS	2.0	_		mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance		C <sub>iss</sub>	<u> </u>	775	_	рF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ f = 1.0 MHz)	Coss	_	96	_	
Transfer Capacitance	,	C <sub>rss</sub>	_	22	_	
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time		<sup>t</sup> d(on)	–	24	_	ns
Rise Time	$(V_{DD} = 250 \text{ V}, \text{ ID} \approx 5.0 \text{ A}, \\ \text{RG} = 12 \Omega, \text{RL} = 50 \Omega,$	t <sub>r</sub>	_	34	_	
Turn-Off Delay Time	VGS(on) = 10 V)	<sup>t</sup> d(off)	_	60	_	
Fall Time	,	t <sub>f</sub>	_	36	_	
Total Gate Charge		Qg	_	27	32	nC
Gate-Source Charge	$(V_{DS} = 320 \text{ V}, I_{D} = 5.0 \text{ A}, V_{GS} = 10 \text{ V})$	Q <sub>gs</sub>	_	3.5	_	
Gate-Drain Charge	vg3 10 V)	Q <sub>gd</sub>	_	14	_	1
SOURCE-DRAIN DIODE CHARAC	TERISTICS*			•		
Forward On–Voltage		V <sub>SD</sub>	_	_	1.4	Vdc
Forward Turn-On Time	(I <sub>S</sub> = 5.0 A, di/dt = 100 A/μs)	ton		**		ns
Reverse Recovery Time		t <sub>rr</sub>	_	_	660	
INTERNAL PACKAGE INDUCTANO	E					
Internal Drain Inductance (Measured from the contact scre (Measured from the drain lead 0.	w on tab to center of die) 25″ from package to center of die)	Ld	_	3.5 4.5	<u>-</u>	nH
Internal Source Inductance (Measured from the source lead	0.25" from package to source bond pad)	L <sub>S</sub>	_	7.5	_	

<sup>\*</sup>Indicates Pulse Test: Pulse Width = 300  $\mu s$  Max, Duty Cycle  $\leq 2.0\%.$  \*\*Limited by circuit inductance.