PRELIMINARY DATA SHEET

NEC

HETERO JUNCTION FIELD EFFECT TRANSISTOR

NE32900

C to Ka BAND SUPER LOW NOISE AMPLIFIER
N-CHANNEL HJ-FET CHIP

DESCRIPTION

NE32900 is Hetero Junction FET chip that utilizes the hetero junction between Si-doped AlGaAs and undoped InGaAs to create high mobility electrons. Its excellent low noise and high associated gain make it suitable for commercial systems, industrial and space applications.

FEATURES

- Super Low Noise Figure & High Associated Gain
  NF = 0.35 dB TYP., G_a = 13.0 dB TYP. at f = 12 GHz
- Gate Length : L_g = 0.2 μm
- Gate Width : W_g = 200 μm

ORDERING INFORMATION

PART NUMBER	QUALITY GRADE
NE32900	Standard (Grade D)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage	V_{DS}	4.0	V
Gate to Source Voltage	V_{GS}	−3.0	V
Drain Current	I_D	I_{DSS}	mA
Total Power Dissipation	P_{tot}*	200	mW
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	−65 to +175	°C

***** Chip mounted on a Alumina heatsink (size: $3 \times 3 \times 0.6^t$)

The information in this document is subject to change without notice.

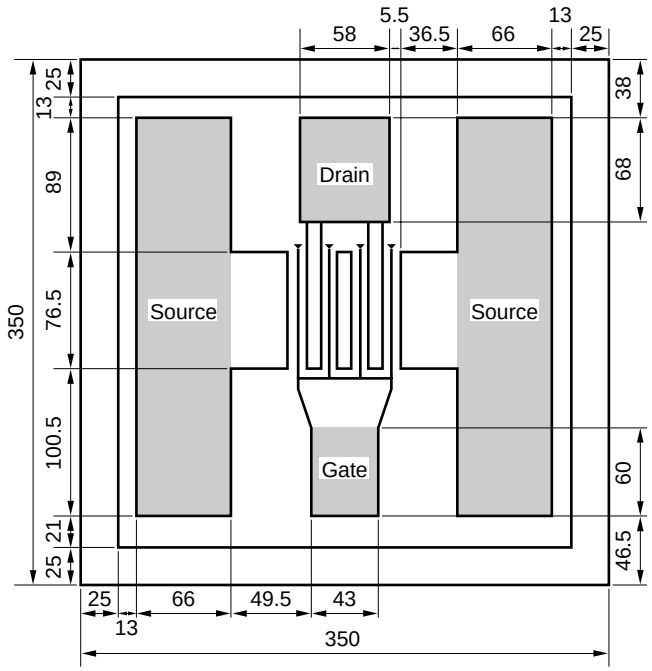
Document No. P12751EJ1V0DS00 (1st edition)
Date Published June 1997 N
Printed in Japan

ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Gate to Source Leak Current	I_{GSO}	–	0.5	10	mA	V_{GS} = –3 V
Saturated Drain Current	I_{DSS}	20	60	90	mA	V_{DS} = 2 V, V_{GS} = 0 V
Gate to Source Cutoff Voltage	$V_{GS(off)}$	–0.2	–0.7	–2.0	V	V_{DS} = 2 V, I_D = 100 μA
Transconductance	g_m	45	60	–	mS	V_{DS} = 2 V, I_D = 10 μA
Thermal Resistance	R_{th}*	–	–	260	°C/W	channel to case
Noise Figure	NF	–	0.35	0.45	dB	V_{DS} = 2 V, I_D = 10 mA, f = 12 GHz
Associated Gain	G_a	11.5	13.0	–	dB	

RF performance is determined by packaging and testing 10 chips per wafer.
Wafer rejection criteria for standard devices is 2 rejects per 10 samples.

CHIP DIMENSIONS (Unit: μm)

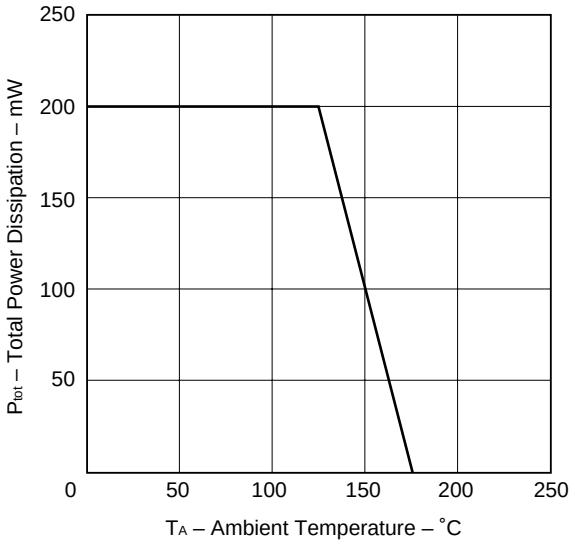


Thickness = 140 μm

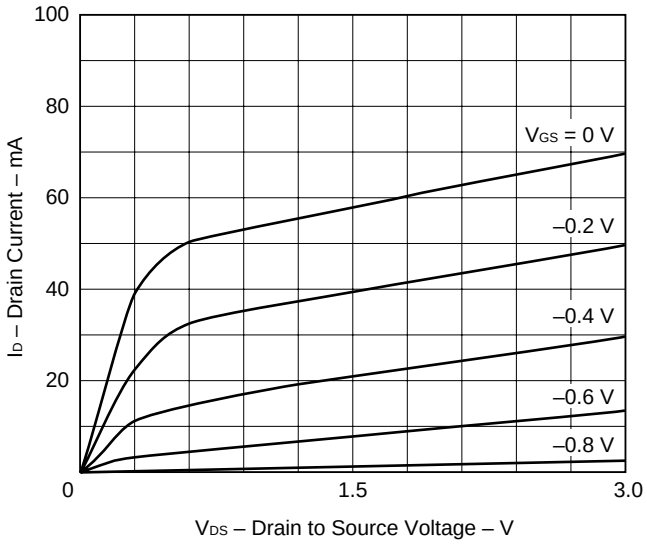
: BONDING AREA

TYPICAL CHARACTERISTICS (T_A = 25 °C)

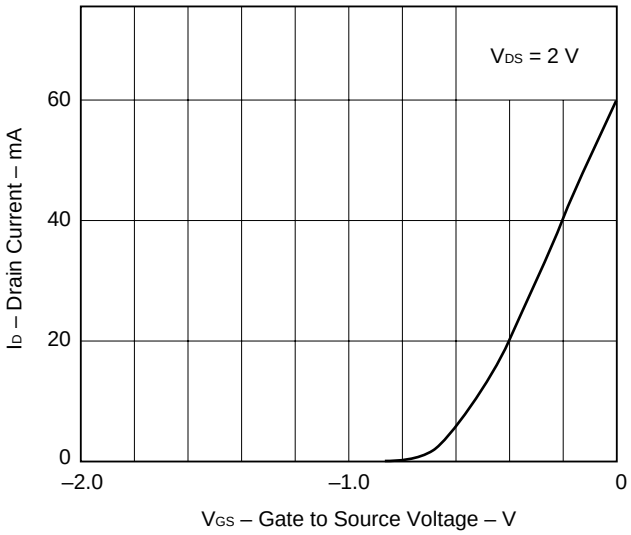
TOTAL POWER DISSIPATION vs.
AMBIENT TEMPERATURE



DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



DRAIN CURRENT vs.
GATE TO SOURCE VOLTAGE

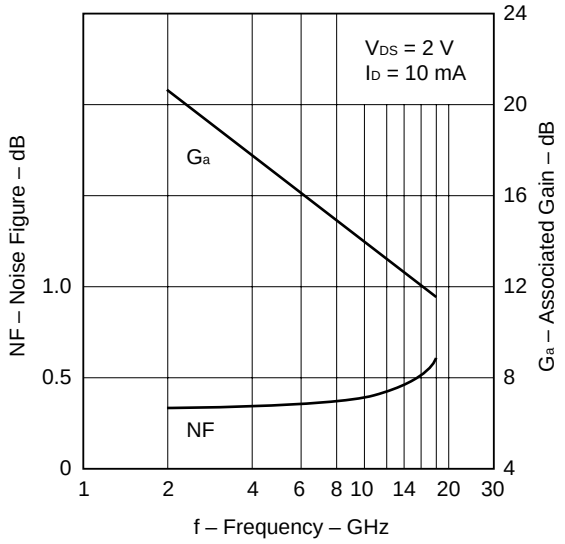


Gain Calculations

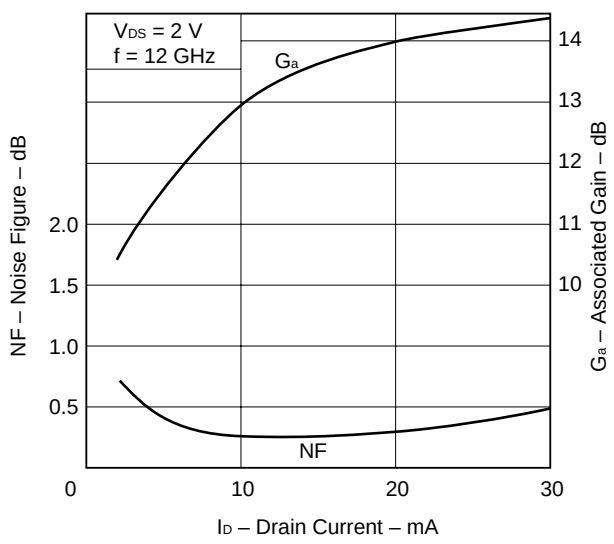
$$MSG. = \frac{|S_{21}|}{|S_{12}|} \qquad K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2\,|S_{12}|\,|S_{21}|}$$

$$MAG. = \frac{|S_{21}|}{|S_{12}|}\,(K \pm \sqrt{K^2 - 1}) \qquad \Delta = S_{11} \bullet S_{22} - S_{21} \bullet S_{12}$$

NOISE FIGURE, ASSOCIATED GAIN vs. FREQUENCY



NOISE FIGURE, ASSOCIATED GAIN vs. DRAIN CURRENT



S-PARAMETER

MAG. AND ANG.

V_{DS} = 2 V, I_D = 10 mA

FREQUENCY	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.
(MHz)		(deg.)		(deg.)		(deg.)		(deg.)
500	0.999	–4	5.53	177	0.007	86	0.562	–3
1000	0.998	–8	5.50	174	0.012	85	0.561	–6
2000	0.995	–16	5.44	168	0.024	80	0.559	–13
3000	0.987	–24	5.39	163	0.035	75	0.556	–19
4000	0.974	–33	5.25	156	0.048	69	0.547	–26
5000	0.962	–40	5.13	151	0.057	66	0.542	–32
6000	0.954	–47	5.02	147	0.066	61	0.535	–37
7000	0.938	–54	4.88	141	0.075	57	0.526	–43
8000	0.921	–60	4.69	137	0.082	53	0.516	–48
9000	0.907	–66	4.55	133	0.089	49	0.509	–53
10000	0.888	–74	4.33	128	0.096	45	0.495	–58
11000	0.877	–76	4.20	125	0.100	42	0.490	–61
12000	0.858	–84	3.99	120	0.106	38	0.477	–66
13000	0.844	–89	3.84	117	0.110	35	0.469	–70
14000	0.828	–94	3.65	113	0.115	32	0.463	–74
15000	0.821	–97	3.55	111	0.117	30	0.459	–76
16000	0.810	–102	3.39	107	0.120	27	0.449	–80
17000	0.792	–106	3.23	104	0.121	25	0.443	–83
18000	0.787	–109	3.12	102	0.123	23	0.443	–84
19000	0.782	–113	3.01	99	0.126	21	0.441	–88
20000	0.780	–116	2.91	97	0.129	19	0.439	–91
21000	0.766	–119	2.79	94	0.131	17	0.431	–93
22000	0.758	–122	2.67	92	0.129	16	0.428	–94
23000	0.757	–125	2.61	90	0.130	14	0.435	–96
24000	0.746	–127	2.50	88	0.132	12	0.426	–99
25000	0.741	–129	2.43	86	0.132	12	0.438	–100
26000	0.742	–131	2.37	84	0.135	9	0.429	–102
27000	0.745	–133	2.28	82	0.130	8	0.428	–105
28000	0.753	–136	2.23	80	0.138	8	0.435	–106
29000	0.749	–138	2.19	78	0.135	7	0.436	–106
30000	0.747	–141	2.12	76	0.133	6	0.429	–109

CHIP HANDLING

DIE ATTACHMENT

Die attach operation can be accomplished with Au-Sn (within a 300 °C – 10 s) performs in a forming gas environment.

Epoxy die attach is not recommend.

BONDING

Bonding wires should be minimum length, semi hard gold wire (3-8 % elongation) 20 microns in diameter.

Bonding should be performed with a wedge tip that has a taper of approximately 15 %. Bonding time should be kept to minimum.

As a general rule, the bonding operation should be kept within a 280 °C, 2 minutes for all bonding wires.

If longer periods are required, the temperature should be lowered.

PRECAUTIONS

The user must operate in a clean, dry environment. The chip channel is glassivated for mechanical protection only and does not preclude the necessity of a clean environment.

The bonding equipment should be periodically checked for sources of surge voltage and should be properly grounded at all times. In fact, all test and handling equipment should be grounded to minimize the possibilities of static discharge.

Avoid high static voltage and electric fields, because this device is Hetero Junction field effect transistor with shottky barrier gate.

CAUTION

The Great Care must be taken in dealing with the devices in this guide.
The reason is that the material of the devices is GaAs (Gallium Arsenide), which is designated as harmful substance according to the law concerned.
Keep the law concerned and so on, especially in case of removal.

[MEMO]

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