

3.6 V OPERATION SILICON RF POWER LD-MOS FET FOR 1.9 GHz 1 W TRANSMISSION AMPLIFIERS

DESCRIPTION

The NE5510179A is an N-channel silicon power MOS FET specially designed as the transmission driver amplifier for 3.6 V GSM 1 800 and GSM 1 900 handsets. Dies are manufactured using NEC's NEWMOS technology (NEC's 0.6 μm WSi gate lateral-diffusion MOS FET) and housed in a surface mount package. The device can deliver 30.0 dBm output power with 50% power added efficiency at 1.9 GHz under the 3.6 V supply voltage, or can deliver 29 dBm output power at 2.8 V by varying the gate voltage as a power control function.

FEATURES

- High output power : $P_{\text{out}} = 30.0$ dBm TYP. ($V_{\text{DS}} = 3.6$ V, $I_{\text{Dset}} = 300$ mA, $f = 1.9$ GHz, $P_{\text{in}} = 22$ dBm)
- High power added efficiency : $\eta_{\text{add}} = 50\%$ TYP. ($V_{\text{DS}} = 3.6$ V, $I_{\text{Dset}} = 300$ mA, $f = 1.9$ GHz, $P_{\text{in}} = 22$ dBm)
- High linear gain : $G_{\text{L}} = 11.0$ dB TYP. ($V_{\text{DS}} = 3.6$ V, $I_{\text{Dset}} = 300$ mA, $f = 1.9$ GHz, $P_{\text{in}} = 10$ dBm)
- Surface mount package : $5.7 \times 5.7 \times 1.1$ mm MAX.
- Single supply : $V_{\text{DS}} = 3.0$ to 6.0 V

APPLICATIONS

- Digital cellular phones : 3.6 V driver amplifier for GSM 1 800/ GSM 1 900 class 1 handsets, or 4.8 V final stage amplifier
- Others : General purpose amplifiers for 1.6 to 2.0 GHz TDMA applications

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
NE5510179A-T1	79A	W1	<ul style="list-style-type: none"> • 12 mm wide embossed taping • Gate pin face the perforation side of the tape • Qty 1 kpcs/reel

Remark To order evaluation samples, consult your NEC sales representative.

Part number for sample order: NE5510179A

Caution Please handle this device at static-free workstation, because this is an electrostatic sensitive device.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	V _{DS}	8.5	V
Gate to Source Voltage	V _{GSO}	5.0	V
Drain Current	I _D	0.5	A
Drain Current (Pulse Test)	I _D ^{Note}	1.0	A
Total Power Dissipation	P _{tot}	1.6	W
Channel Temperature	T _{ch}	125	°C
Storage Temperature	T _{stg}	-65 to +125	°C

Note Duty Cycle ≤ 50%, T_{on} ≤ 1 ms

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain to Source Voltage	V _{DS}		3.0	3.6	6.0	V
Gate to Source Voltage	V _{GSO}		0	2.0	3.0	V
Drain Current (Pulse Test)	I _D	Duty Cycle ≤ 50%, T _{on} ≤ 1 ms	-	0.45	0.7	A
Input Power	P _{in}	f = 1.9 GHz, V _{DS} = 3.6 V	20	22	25	dBm

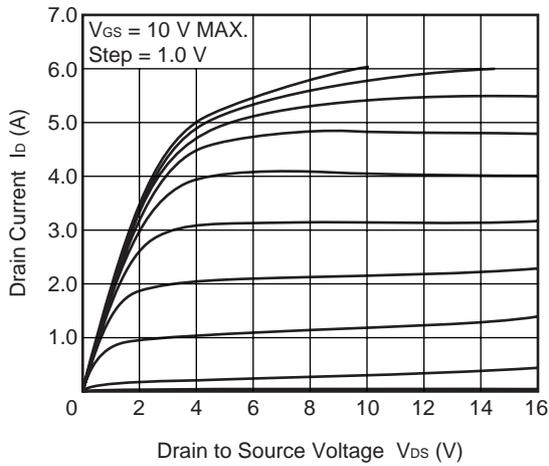
ELECTRICAL CHARACTERISTICS (T_A = +25°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source Leak Current	I _{GSO}	V _{GSS} = 5.0 V	-	-	100	nA
Saturated Drain Current (Zero Gate Voltage Drain Current)	I _{DSS}	V _{DSS} = 8.5 V	-	-	100	nA
Gate Threshold Voltage	V _{th}	V _{DS} = 4.8 V, I _{DS} = 1 mA	1.0	1.4	2.0	V
Transconductance	g _m	V _{DS} = 4.8 V, I _{DS} = 400 mA	-	840	-	mS
Drain to Source Breakdown Voltage	BV _{DS}	I _{DSS} = 10 μA	20	24	-	V
Thermal Resistance	R _{th}	Channel to Case	-	10	-	°C/W
Linear Gain	G _L	f = 1.9 GHz, P _{in} = 10 dBm, V _{DS} = 3.6 V, I _{Dset} = 300 mA, Note	-	11.0	-	dB
Output Power	P _{out}	f = 1.9 GHz, P _{in} = 22 dBm, V _{DS} = 3.6 V, I _{Dset} = 300 mA, Note	29.0	30.0	-	dBm
Operating Current	I _{op}	V _{DS} = 3.6 V, I _{Dset} = 300 mA, Note	-	450	-	mA
Power Added Efficiency	η _{add}	V _{DS} = 3.6 V, I _{Dset} = 300 mA, Note	43	50	-	%

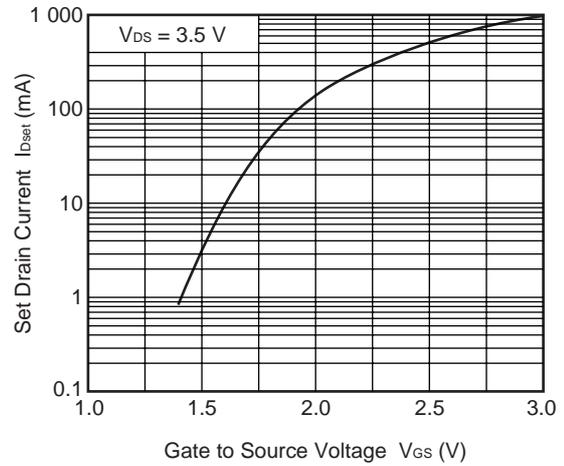
Note DC performance is 100% testing. RF performance is testing several samples per wafer.
Wafer rejection criteria for standard devices is 1 reject for several samples.

TYPICAL CHARACTERISTICS (T_A = +25°C)

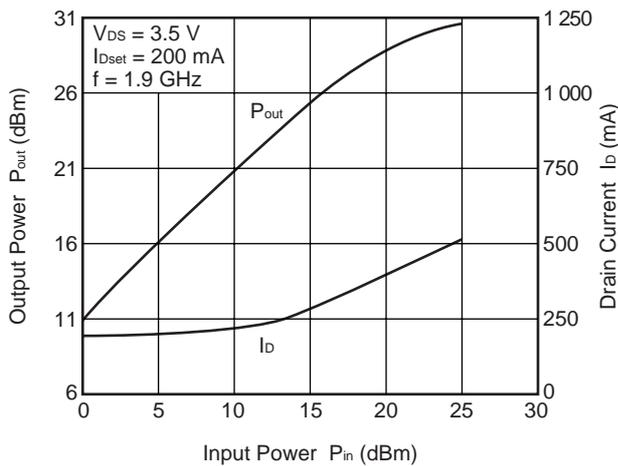
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



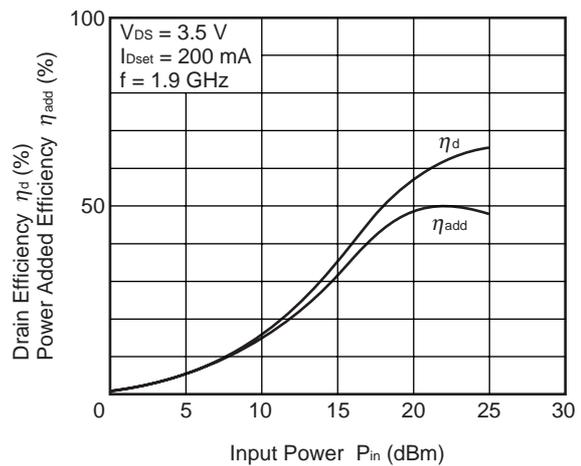
SET DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



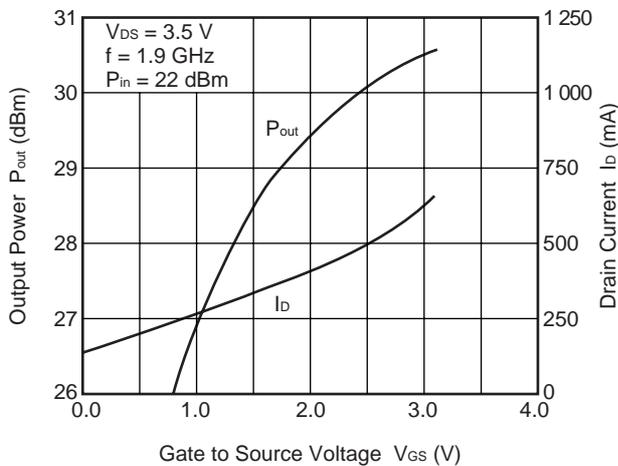
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER



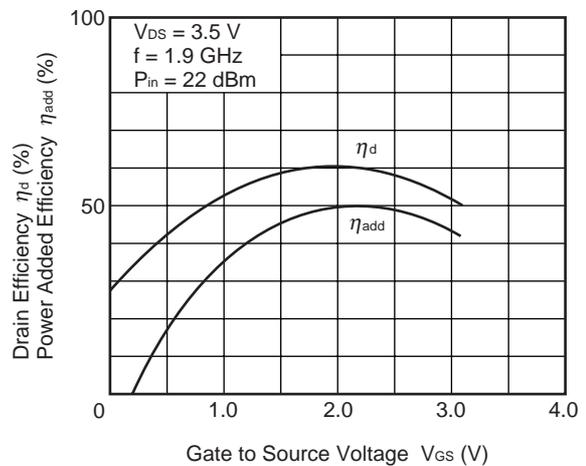
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



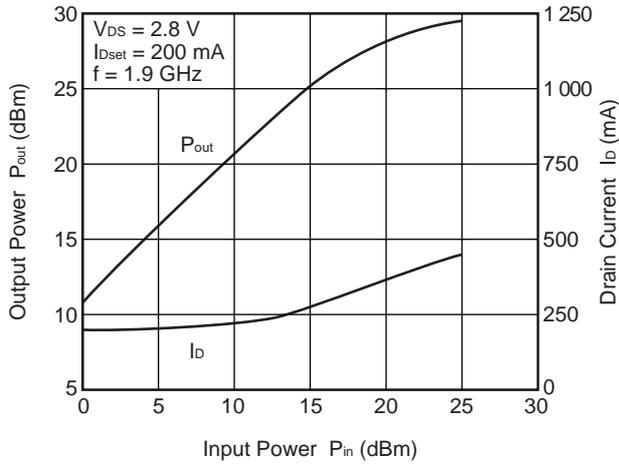
OUTPUT POWER, DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



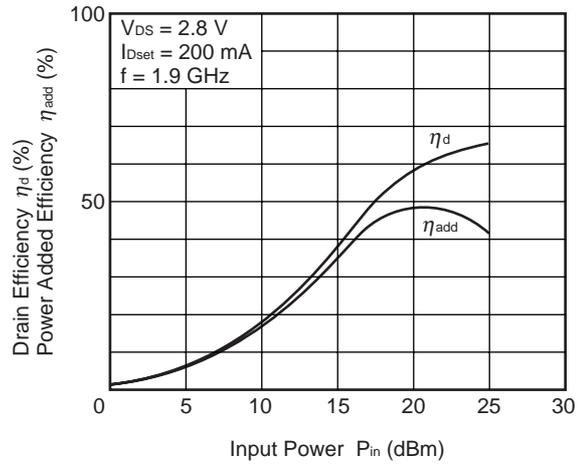
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. GATE TO SOURCE VOLTAGE



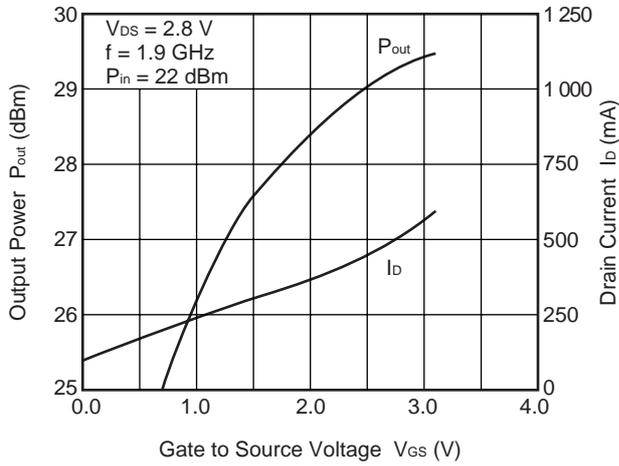
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER



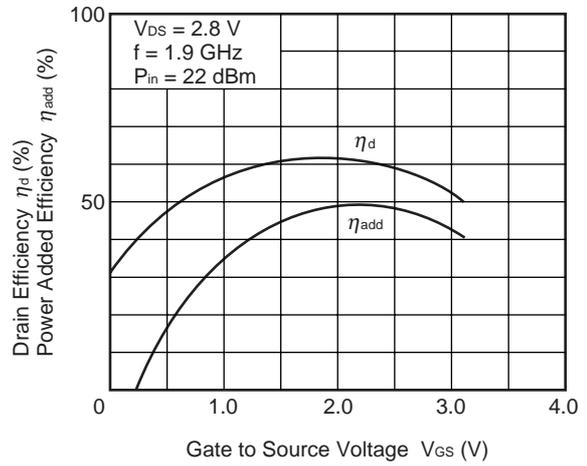
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



OUTPUT POWER, DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. GATE TO SOURCE VOLTAGE



Remark The graphs indicate nominal characteristics.

S-PARAMETERS

Test Conditions: $V_{DS} = 3.5\text{ V}$, $I_{Dset} = 200\text{ mA}$

Frequency GHz	S ₁₁			S ₂₁			S ₁₂		S ₂₂		MAG ^{Note}	MSG ^{Note}	K
	MAG.	ANG.	dB	MAG.	ANG.	dB	MAG.	ANG.	MAG.	ANG.	dB	dB	
0.1	0.834	-121.1	22.8	13.84	111.3	-30.2	0.031	23.5	0.656	-154.0		26.5	
0.2	0.809	-148.1	17.5	7.49	93.6	-29.6	0.033	6.7	0.717	-164.8		23.6	
0.3	0.809	-158.2	13.9	4.96	84.6	-29.6	0.033	-2.6	0.741	-168.5		21.8	
0.4	0.812	-163.4	11.3	3.67	77.1	-29.9	0.032	-8.3	0.756	-170.5		20.6	0.07
0.5	0.821	-166.8	9.2	2.90	71.2	-29.9	0.032	-13.3	0.779	-171.6		19.6	0.10
0.6	0.829	-169.4	7.3	2.32	66.2	-30.8	0.029	-17.2	0.792	-172.7		19.0	0.24
0.7	0.837	-171.4	5.8	1.96	61.7	-31.4	0.027	-18.3	0.807	-173.4		18.6	0.34
0.8	0.854	-173.4	4.2	1.63	57.3	-31.7	0.026	-22.7	0.818	-174.6		18.0	0.38
0.9	0.856	-175.0	3.1	1.43	52.6	-32.4	0.024	-24.6	0.832	-175.5		17.8	0.50
1.0	0.865	-176.7	1.8	1.23	50.3	-32.8	0.023	-24.6	0.841	-176.7		17.3	0.59
1.1	0.876	-178.4	0.8	1.10	46.2	-33.6	0.021	-29.3	0.856	-177.5		17.2	0.61
1.2	0.880	180.0	-0.4	0.96	44.3	-34.4	0.019	-27.9	0.863	-178.9		17.0	0.83
1.3	0.888	178.0	-1.3	0.86	39.9	-34.9	0.018	-28.1	0.870	179.8		16.8	0.90
1.4	0.895	176.5	-2.2	0.78	38.1	-35.4	0.017	-29.1	0.880	178.4		16.6	0.91
1.5	0.899	174.9	-3.0	0.71	34.2	-35.4	0.017	-31.7	0.888	177.6		16.2	0.89
1.6	0.902	172.9	-3.7	0.65	33.3	-37.1	0.014	-35.2	0.893	175.8	13.5		1.27
1.7	0.901	170.9	-4.9	0.57	29.9	-37.7	0.013	-28.2	0.894	174.7	11.4		1.75
1.8	0.912	169.3	-5.4	0.54	27.1	-39.2	0.011	-23.9	0.908	172.5	12.2		1.66
1.9	0.908	167.0	-6.2	0.49	24.4	-40.0	0.010	-23.0	0.909	171.2	10.5		2.29
2.0	0.911	165.1	-6.6	0.47	23.8	-40.0	0.010	-15.1	0.919	169.5	11.1		1.98
2.1	0.913	162.2	-7.5	0.42	20.5	-43.1	0.007	-3.7	0.906	167.8	8.6		4.25
2.2	0.914	160.8	-8.2	0.39	19.1	-44.4	0.006	-4.1	0.919	166.0	8.5		4.63
2.3	0.920	158.3	-9.1	0.35	15.2	-44.4	0.006	6.0	0.920	163.5	7.9		4.77
2.4	0.914	156.1	-9.1	0.35	13.4	-41.9	0.008	13.9	0.926	162.0	8.3		3.34
2.5	0.918	153.5	-10.2	0.31	13.0	-44.4	0.006	15.1	0.925	160.6	7.0		5.26
2.6	0.921	151.5	-10.5	0.30	12.2	-43.1	0.007	31.8	0.920	157.9	6.6		4.70
2.7	0.918	149.1	-11.7	0.26	9.5	-43.1	0.007	45.0	0.919	155.7	5.0		5.87
2.8	0.920	147.1	-11.4	0.27	4.8	-40.0	0.010	48.1	0.940	153.5	7.6		2.45
2.9	0.921	145.0	-12.4	0.24	6.4	-40.9	0.009	62.0	0.928	152.4	5.3		4.02
3.0	0.925	142.9	-12.4	0.24	4.8	-40.0	0.010	57.7	0.938	150.2	6.6		2.75

Note When $K \geq 1$, the MAG (Maximum Available Gain) is used. $MAG = \left| \frac{S_{21}}{S_{12}} \right| (K - \sqrt{K^2 - 1})$

When $K < 1$, the MSG (Maximum Stable Gain) is used. $MSG = \left| \frac{S_{21}}{S_{12}} \right|$, $K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 \cdot |S_{12}| \cdot |S_{21}|}$,

$$\Delta = S_{11} \cdot S_{22} - S_{21} \cdot S_{12}$$

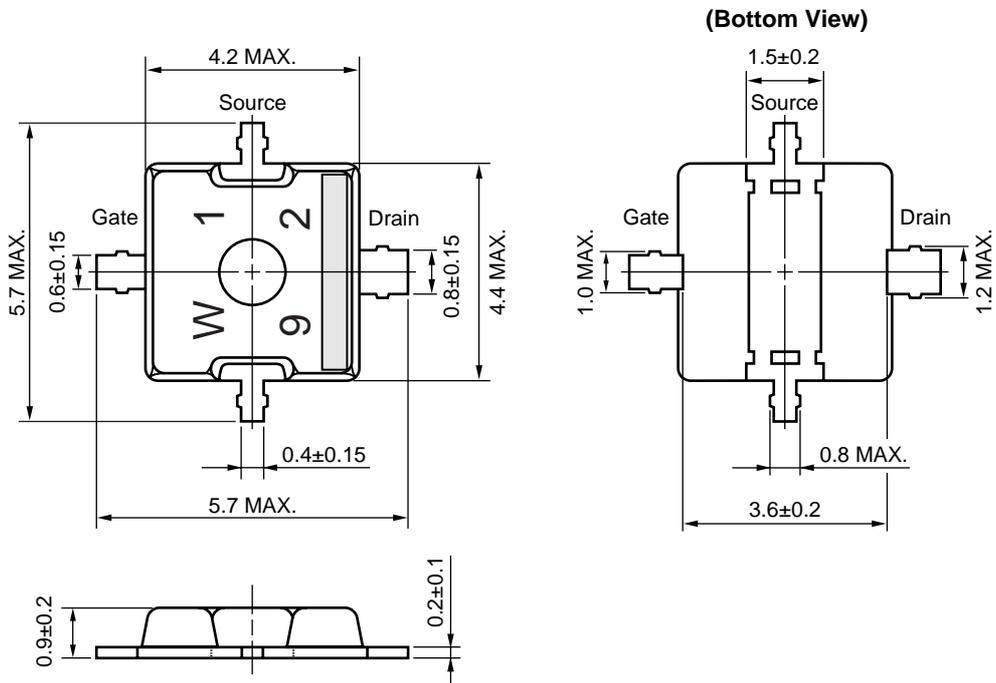
LARGE SIGNAL IMPEDANCE ($V_{DS} = 3.5\text{ V}$, $I_{Dset} = 200\text{ mA}$, $P_{in} = 22\text{ dBm}$)

f (GHz)	Z _{in} (Ω)	Z _{OL} (Ω) ^{Note}
1.9	TBD	TBD

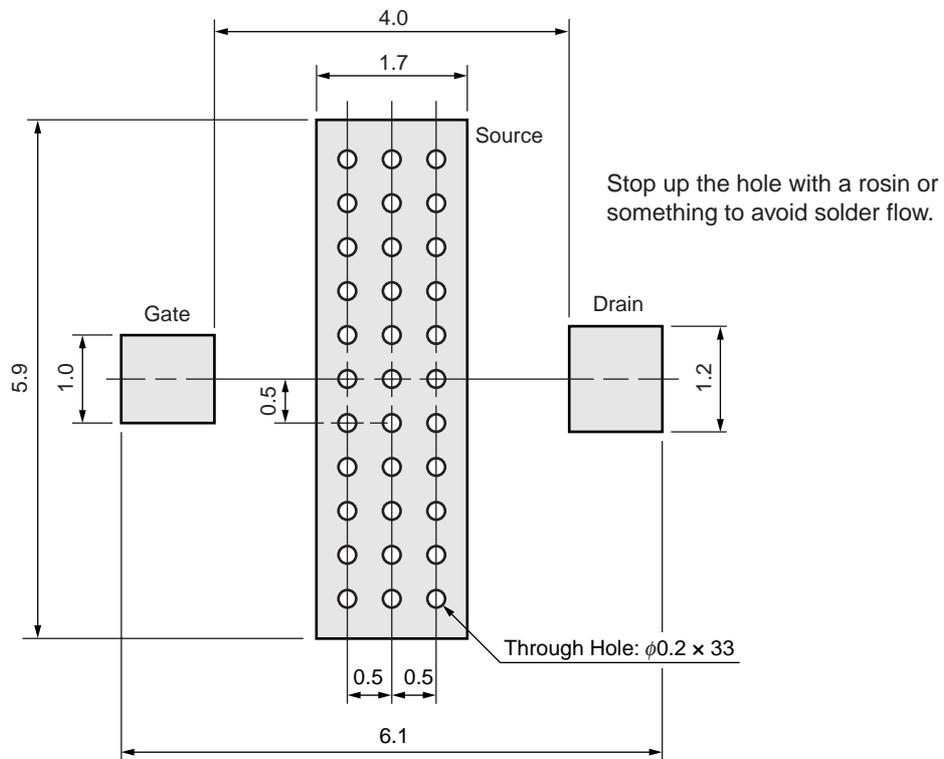
Note Z_{OL} is the conjugate of optimum load impedance at given voltage, idling current, input power and frequency.

PACKAGE DIMENSIONS

79A (UNIT: mm)



79A PACKAGE RECOMMENDED P.C.B. LAYOUT (UNIT: mm)



RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below, Time: 30 seconds or less (at 210°C or higher), Count: 2 times or less, Exposure: limit: None ^{Note}	IR35-00-2
Partial Heating	Pin temperature: 260°C or below, Time: 5 seconds or less (per pin row) Exposure: limit: None ^{Note}	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

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