PRELIMINARY DATA SHEET

NEC

N-CHANNEL GaAs MESFET
NES1823P-100

100W L-BAND PUSH-PULL POWER GaAs MESFET

DESCRIPTION

The NES1823P-100 is a 100 W push-pull type GaAs MESFET designed for high power transmitter applications for IMT-2000 and PCS/PCN base station systems. It is capable of delivering 100 watts of output power with high linear gain, high efficiency and excellent distortion. Its primary band is 1.8 to 2.3 GHz with different maching.

The device employs Tungsten Silicide gates, via holes, plated heat sink, and silicon dioxide and nitride passivation for superior performance, thermal characteristics, and reliability.

Reliability and performance uniformity are assured by NEC's stringent quality and control procedures.

FEATURES

- Push-pull type N-channel GaAs MESFET
- High Output Power : 100 W TYP.
- High Linear Gain : 11.0 dB TYP.
- High Drain Efficiency : 50 % TYP. @V_{DS} = 10 V, I_{Dset} = 6 A, f = 2.2 GHz

ORDERING INFORMATION (PLAN)

Part Number	Package	Supplying Form
NES1823P-100	T-92	ESD protective envelope

Remark To order evaluation samples, please contact your local NEC sales office.
(Part number for sample order: NES1823P-100)

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Operation in excess of any one of these parameters may result in permanent damage.

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	15	V
Gate to Source Voltage	V_{GSO}	–7	V
Drain Current	I_D	76	A
Gate Current	I_G	440	mA
Total Power Dissipation	P_T	220 Note	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–65 to +175	°C

Note T_C = 25°C

Caution Please handle this device at static-free workstation, because this is an electrostatic sensitive device.

Document No. P13839EJ1V0DS00 (1st edition)
Date Published November 1998 N CP(K)
Printed in Japan

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Drain to Source Voltage	V_{DS}			10.0	10.0	V
Gain Compression	Gcomp				3.0	dB
Channel Temperature	T_{ch}				+150	°C
Set Drain Current[Note 1]	I_{Dset}			6.0	8.0	A
Gate Resistance[Note 2]	R_g			10	12.5	Ω

Notes 1. I_{Dset} = 3.0 A each drain, V_{DS} = 10 V, RF OFF.

2. R_g is the series resistance between the gate supply and FET gate.

ELECTRICAL CHARACTERISTICS (T_A = +25°C)

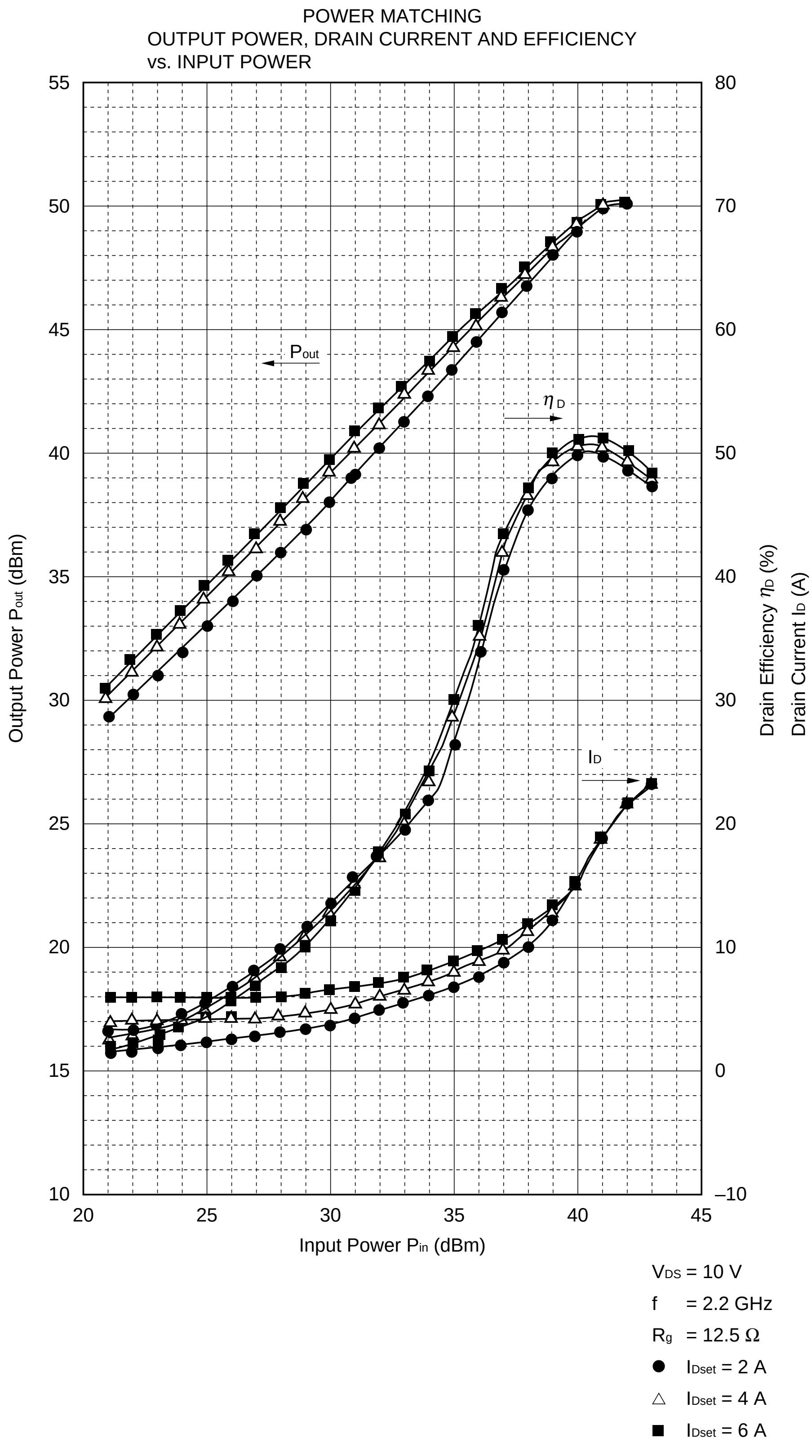
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturated Drain Current	I_{DSS}	V_{DS} = 2.5 V, V_{GS} = 0 V		76		A
Pinch-off Voltage	V_p	V_{DS} = 2.5 V, I_{DS} = 330 mA	–4.0	–2.6		V
Thermal Resistance	R_{th}	Channel to Case		0.6	0.8	°C/W
Output Power	P_{out}	f = 2.2 GHz, V_{DS} = 10 V P_{in} = +42.5 dBm, R_g = 12.5 Ω I_{Dset} = 6.0 A Total (RF OFF)[Note]	49.0	50.0		dBm
Drain Current	I_D			20.0	32.5	A
Drain Efficiency	η_D			50		%
Linear Gain	G_L		9.0	11.0		dB

Note I_{Dset} = 3.0 A each drain

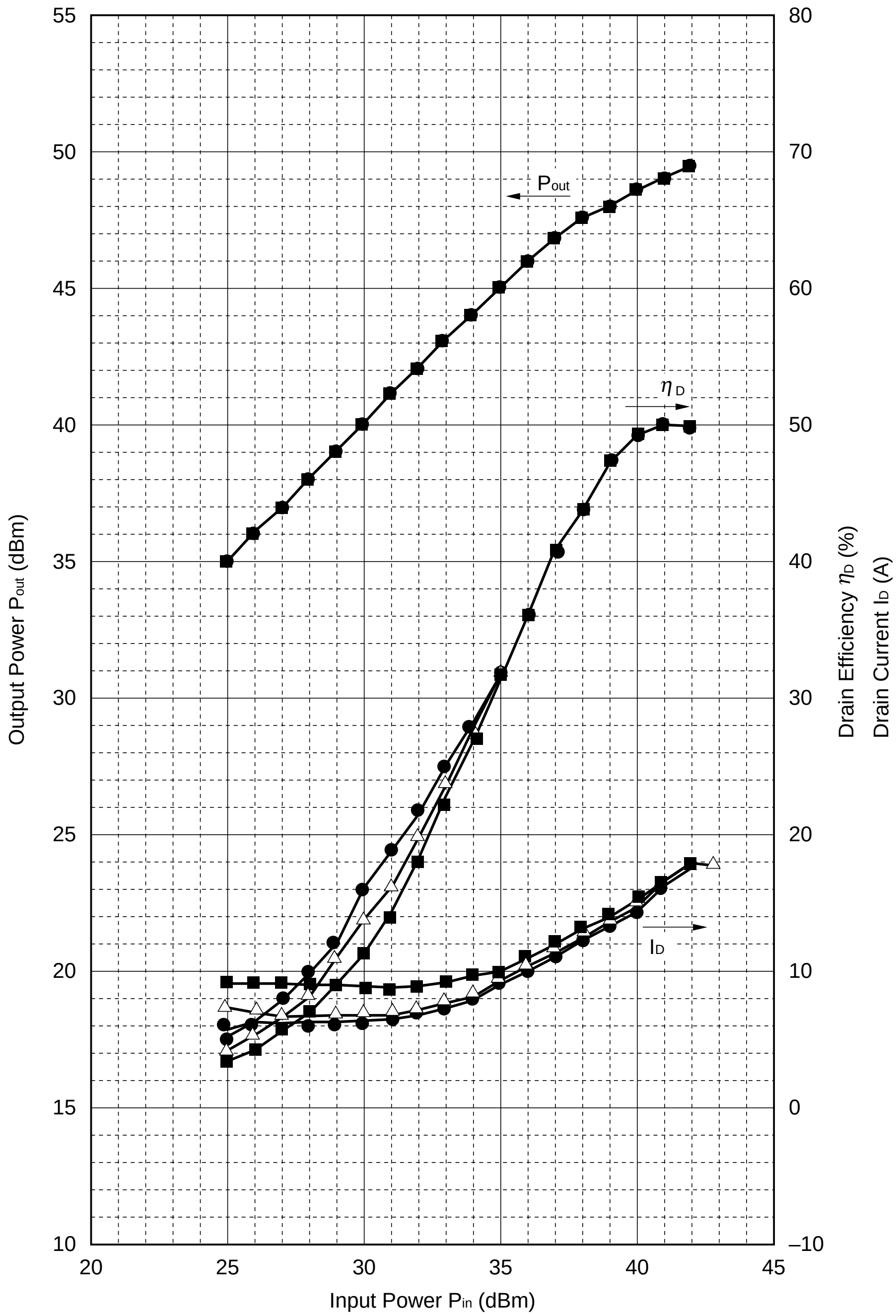
TYPICAL CHARACTERISTICS (T_A = +25°C)

POWER MATCHING AND IM_3 MATCHING

NEC produces two type matching circuits, power matching and IM_3 matching. Power matching circuit is used our production line. And the IM_3 matching circuit is useful for the customers to design the special tuning application. The power matching is designed as this, input impedance is gain-matching, output is matched with power matching impedance which is calculated with large signal simulation model. The IM_3 matching is designed as this, input impedance is matched to the impedance which has the direction of decreasing S_{21} phase-shift, output impedance is matched to the almost same as the efficiency matching impedance. Those typical RF data are shown as this, G_L = 10.2 dB P_{out} = 50.0 dBm IM_3 = –28 dBc at power matching, G_L = 10.0 dB P_{out} = 49.3 dBm IM_3 = –31 dBc at IM_3 matching (@2 tone P_{out} = 40 dBm).

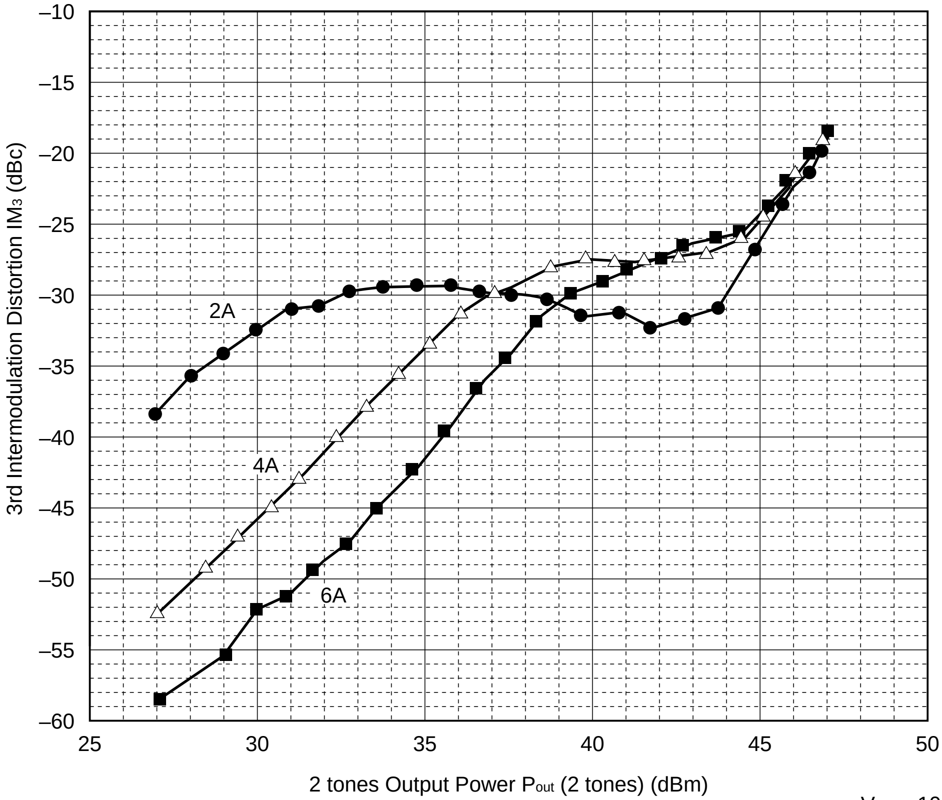

POWER MATCHING
OUTPUT POWER, DRAIN CURRENT AND EFFICIENCY
vs. INPUT POWER
55
50
45
40
35
30
25
20
15
10
80
70
60
50
40
30
20
10
0
–10
20
25
30
35
40
45
Pout
η D
ID
Output Power Pout (dBm)
Drain Efficiency ηD (%)
Drain Current ID (A)
Input Power Pin (dBm)
VDS = 10 V
f = 2.2 GHz
Rg = 12.5 Ω
● IDset = 2 A
△ IDset = 4 A
■ IDset = 6 A

DISTORTION MATCHING
OUTPUT POWER, DRAIN CURRENT AND EFFICIENCY
vs. INPUT POWER

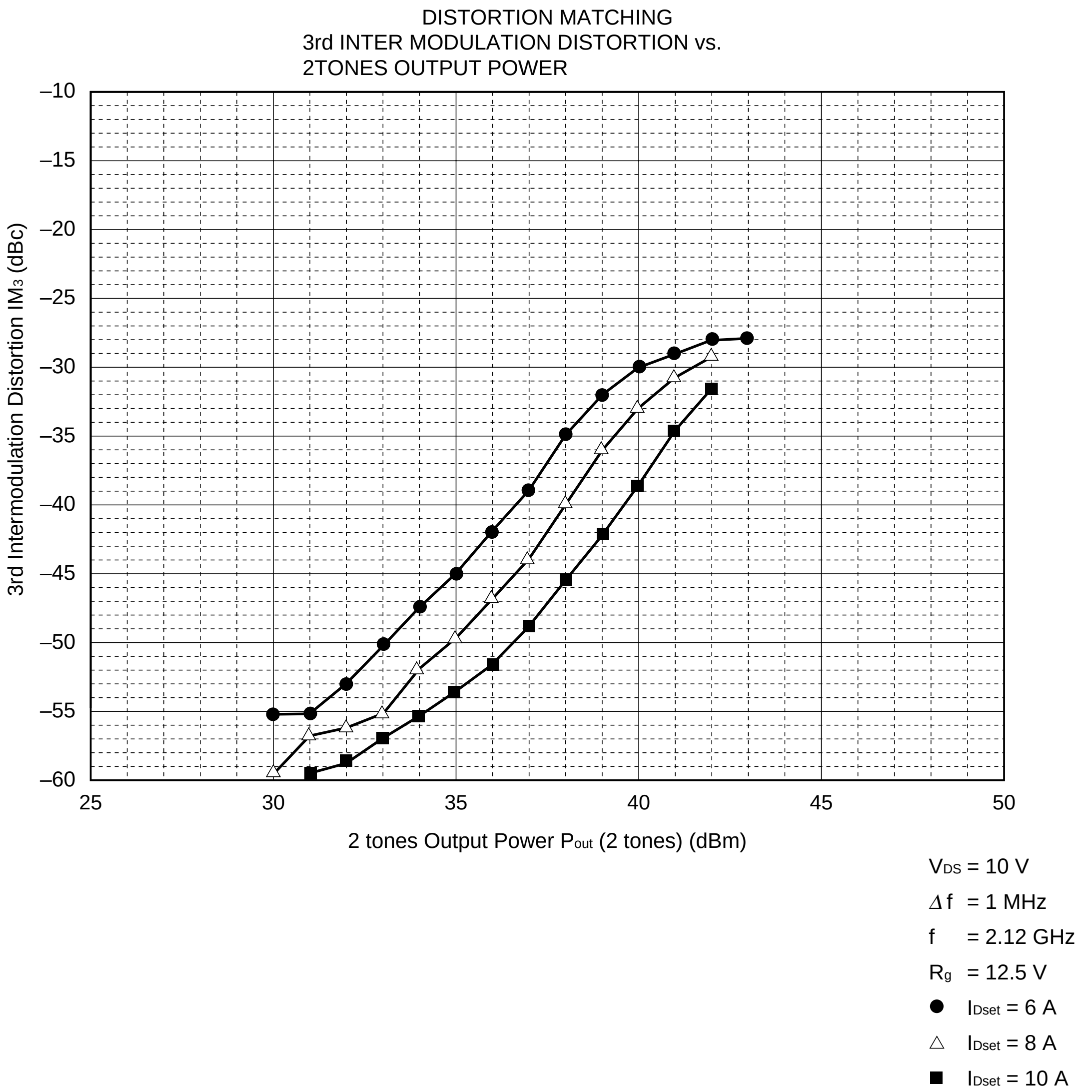


V_{DS} = 10 V
f = 2.12 GHz
R_g = 12.5 Ω
● I_{Dset} = 6 A
△ I_{Dset} = 8 A
■ I_{Dset} = 10 A

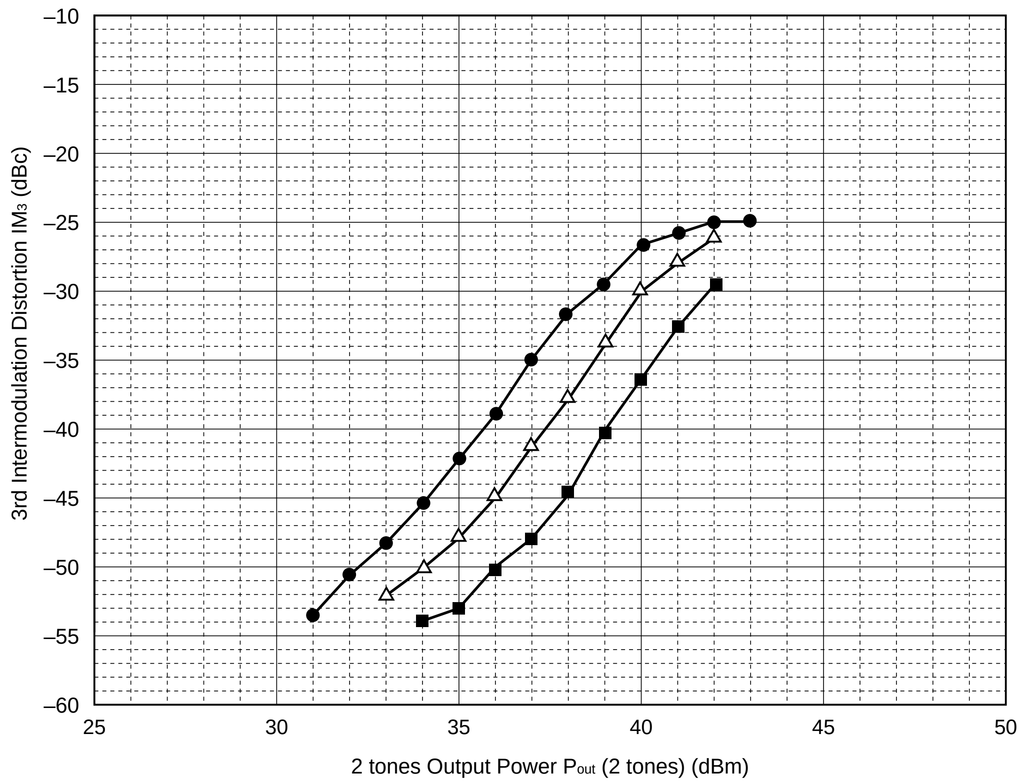
POWER MATCHING
3rd INTERMODULATION DISTORTION vs.
2 TONES OUTPUT POWER



V_{DS} = 10 V
Δf = 1 MHz
f = 2.2 GHz
R_g = 12.5 Ω
● I_{Dset} = 2 A
△ I_{Dset} = 4 A
■ I_{Dset} = 6 A


DISTORTION MATCHING
3rd INTER MODULATION DISTORTION vs.
2TONES OUTPUT POWER
3rd Intermodulation Distortion IM3 (dBc)
–10
–15
–20
–25
–30
–35
–40
–45
–50
–55
–60
25
30
35
40
45
50
2 tones Output Power Pout (2 tones) (dBm)
VDS = 10 V
Δf = 1 MHz
f = 2.12 GHz
Rg = 12.5 V
IDset = 6 A
IDset = 8 A
IDset = 10 A

DISTORTION MATCHING
3rd INTER MODULATION DISTORTION vs.
2TONES OUTPUT POWER



V_{DS} = 10 V
Δf = 20 MHz
f = 2.12 GHz
R_g = 12.5 Ω
● I_{Dset} = 6 A
△ I_{Dset} = 8 A
■ I_{Dset} = 10 A

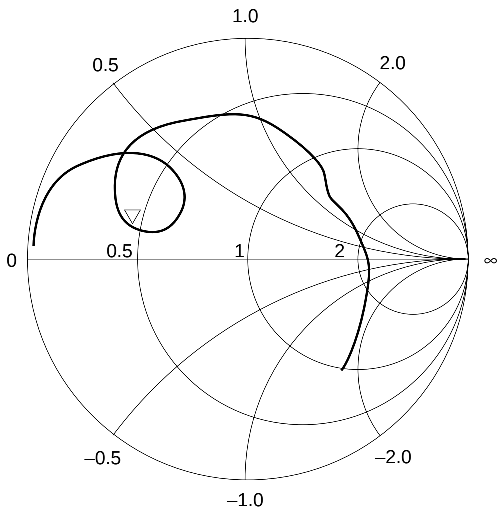
S-Parameters

V_{DS} = 10 V, I_{Dset} = 3 A each drain

START 1 GHz, STOP 3 GHz, STEP 40 MHz

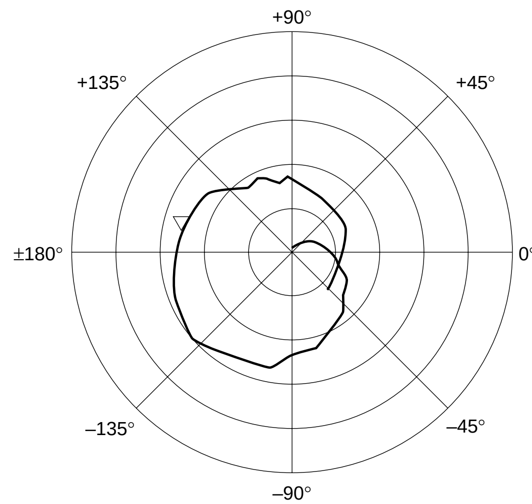
Marker 2.2 GHz

S_{11}



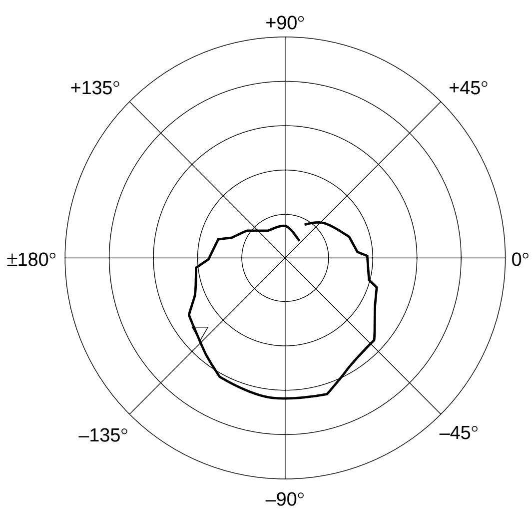
$R_{max.}$ = 1

S_{12}



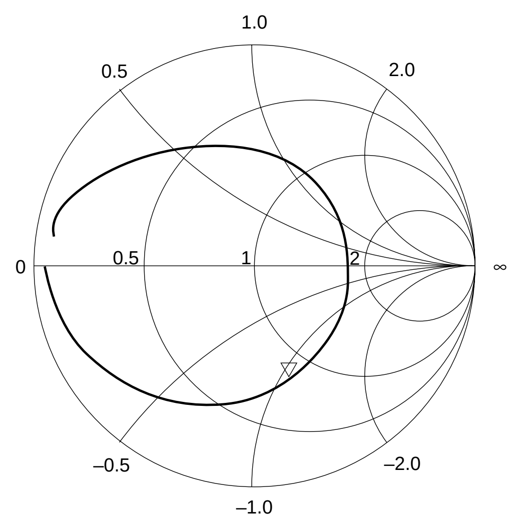
$R_{max.}$ = 0.1

S_{21}



$R_{max.}$ = 5

S_{22}



$R_{max.}$ = 1

S-Parameters

V_{DS} = 10 V, I_{Dset} = 3 A each drain

FREQUENCY	S_{11}		S_{21}		S_{12}		S_{22}	
GHz	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.
1.000	0.959	173.5	0.857	65.1	0.006	62.5	0.943	171.2
1.040	0.959	172.7	0.537	58.8	0.006	57.4	0.924	166.7
1.080	0.956	171.7	0.478	57.7	0.006	53.7	0.922	165.7
1.120	0.956	170.8	0.429	58.5	0.007	51.0	0.914	164.2
1.160	0.956	170.8	0.419	59.5	0.007	48.3	0.904	162.7
1.200	0.950	168.7	0.408	62.7	0.008	47.1	0.898	161.5
1.240	0.946	167.5	0.424	60.9	0.008	43.5	0.880	159.8
1.280	0.941	166.2	0.416	66.8	0.009	43.8	0.866	158.2
1.320	0.941	164.8	0.475	68.3	0.009	37.8	0.851	156.4
1.360	0.935	163.3	0.540	68.3	0.010	34.8	0.832	154.7
1.400	0.927	161.7	0.577	67.2	0.012	32.1	0.814	152.8
1.440	0.920	159.9	0.728	66.4	0.012	28.6	0.794	150.9
1.480	0.912	158.1	0.780	59.2	0.014	20.2	0.776	148.9
1.520	0.903	156.0	0.956	55.2	0.015	18.9	0.758	146.8
1.560	0.890	153.9	1.001	46.2	0.017	9.6	0.739	144.5
1.600	0.876	151.5	1.183	41.6	0.018	7.7	0.720	142.0
1.640	0.858	149.1	1.262	30.6	0.021	–1.8	0.701	139.5
1.680	0.839	146.6	1.364	24.7	0.022	–8.4	0.683	136.7
1.720	0.815	143.8	1.542	16.7	0.025	–18.3	0.663	133.6
1.760	0.789	141.2	1.585	6.3	0.028	–25.1	0.644	130.0
1.800	0.756	138.1	1.823	3.4	0.030	–36.7	0.625	125.8
1.840	0.719	135.1	1.968	–11.4	0.036	–45.7	0.606	120.5
1.880	0.674	132.1	2.157	–16.4	0.038	–58.5	0.583	113.6
1.920	0.616	129.1	2.379	–28.8	0.044	–74.2	0.563	104.6
1.960	0.548	127.3	2.757	–40.5	0.045	–85.5	0.535	91.7
2.000	0.474	127.6	2.806	–54.6	0.054	–103.2	0.499	74.1
2.040	0.405	132.9	3.193	–70.0	0.055	–120.7	0.461	50.3
2.080	0.371	144.4	3.181	–85.4	0.059	–140.4	0.436	19.8
2.120	0.403	156.0	3.141	–103.6	0.058	–159.5	0.443	–14.0
2.160	0.477	160.5	3.069	–118.7	0.054	–179.6	0.483	–44.9
2.200	0.553	159.4	2.740	–133.2	0.051	168.1	0.543	–69.8
2.240	0.622	155.8	2.545	–150.0	0.048	147.2	0.605	–89.0
2.280	0.664	150.3	2.246	–157.0	0.042	135.8	0.660	–103.5
2.320	0.693	144.6	2.008	–175.7	0.036	123.9	0.708	–115.0
2.360	0.712	138.7	1.732	–178.2	0.038	114.5	0.749	–124.2
2.400	0.719	132.7	1.576	165.7	0.031	100.7	0.783	–131.9
2.440	0.723	127.3	1.333	161.8	0.033	94.9	0.804	–136.9
2.480	0.721	120.8	1.181	156.5	0.029	80.3	0.823	–142.7
2.520	0.713	114.1	1.131	149.7	0.028	74.3	0.848	–147.4
2.560	0.701	106.5	0.887	145.0	0.028	65.5	0.860	–151.8
2.600	0.684	98.3	0.965	142.0	0.028	46.9	0.875	–155.2
2.640	0.661	88.7	0.751	135.7	0.026	44.9	0.882	–158.4
2.680	0.632	78.0	0.851	134.8	0.027	27.6	0.894	–161.5
2.720	0.594	65.6	0.727	125.7	0.026	18.4	0.900	–163.8
2.760	0.542	51.8	0.735	119.7	0.023	3.4	0.907	–166.2
2.800	0.483	40.7	0.650	119.2	0.022	–5.7	0.915	–168.7
2.840	0.499	29.6	0.714	109.0	0.020	–7.0	0.917	–170.4
2.880	0.530	10.9	0.636	106.7	0.023	–15.0	0.923	–172.2
2.920	0.555	–9.1	0.689	94.9	0.023	–24.8	0.928	–174.0
2.960	0.587	–28.3	0.654	88.7	0.022	–36.4	0.931	–175.7
3.000	0.625	–46.2	0.625	72.9	0.024	–47.5	0.932	–177.1

CIRCUIT DESIGN

The matching circuit of package inside consists of bond-wire, chip-capacitor and microstrip line on the alumina substrate. The package-lead impedance is designed as 25 Ω connecting to the external matching circuit, in the external circuit design, the microstrip line impedance is 25 Ω, conjugate with package impedance, then the impedance is connected to balun, it is 1:2 balun structure, finally connected to 50 Ω. Balun technology has some advantage over single-ended device, minimize matching-loss with decrease of impedance change ratio and cancel the even mode harmonic frequency for IM_3 performance. The balun circuit is employed for this product.

BALUN DESIGN

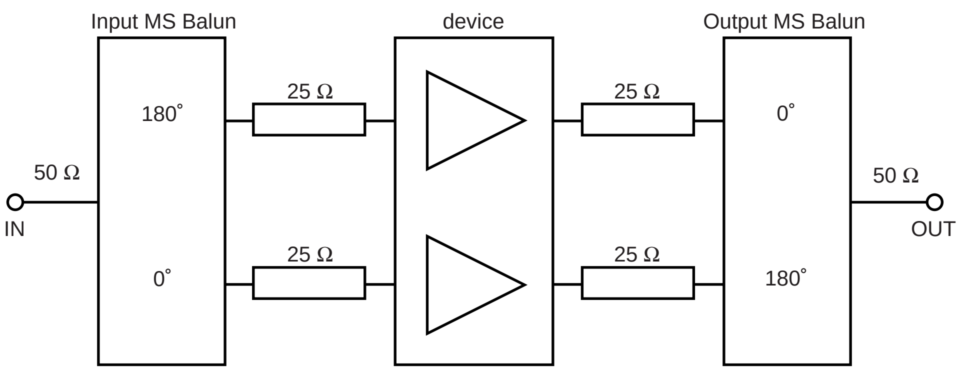
The balun design is the key for these high power push-pull structure device. NEC designed low insertion loss microstrip balun for this product. What is the reason of our choice? One is the repeatability of assembly, and the other is its performance. Microstrip balun performance tolerance is small because of its simple structure. So the balun performance is stable and repeatable between NEC and customers. And its insertion loss is 0.2 dB less than coaxial balun 0.3 dB, also Its band width is better than coaxial balun. The microstrip balun is consists of microstrip pattern and cavity, therefore its insertion loss and band width due to its parameter design. Those parameters are optimized with simuration. : (substrate duroid εr = 2.2 t = 0.8 mm)

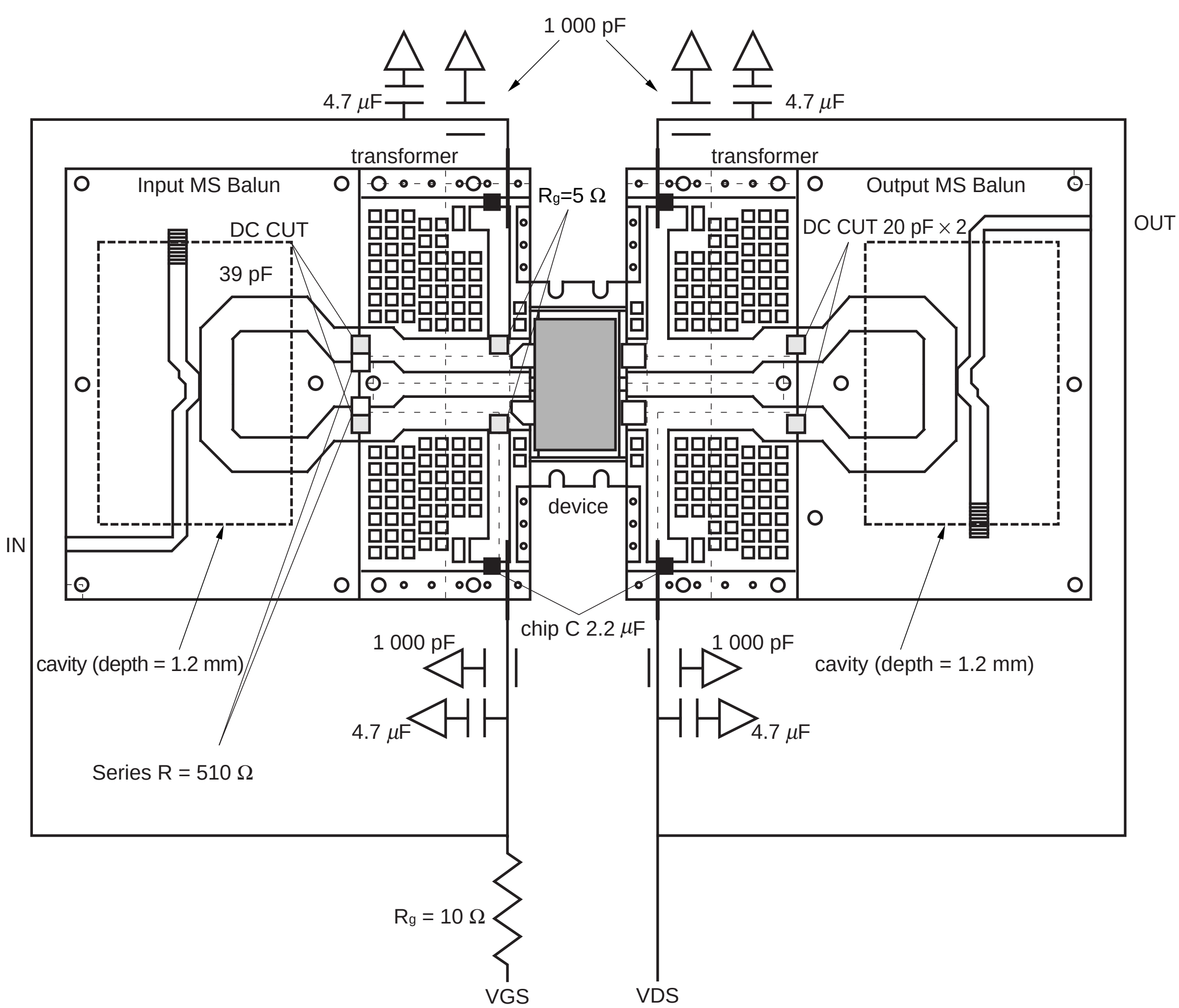
Then the phase difference between two ports is 180° ±4, insertion loss is 0.2 dB from 1 to 3 GHz.

DC STABILITY (AVOID OSCILLATION)

The function of DC-cut capacitor arranged between transformer and microstrip balun is avoid DC oscillation. When the gate is pinch-off, a few pinch-off voltage (VP) difference of each port occur the loop current, then start DC oscillation in the area of pinch-off. Because of this reasons, the DC-cut capacitor is need to this microstrip balun assemble. Additionally, the ground of transformer substate is effective to DC oscillation, so that five screws are arranged at the middle of substrate.

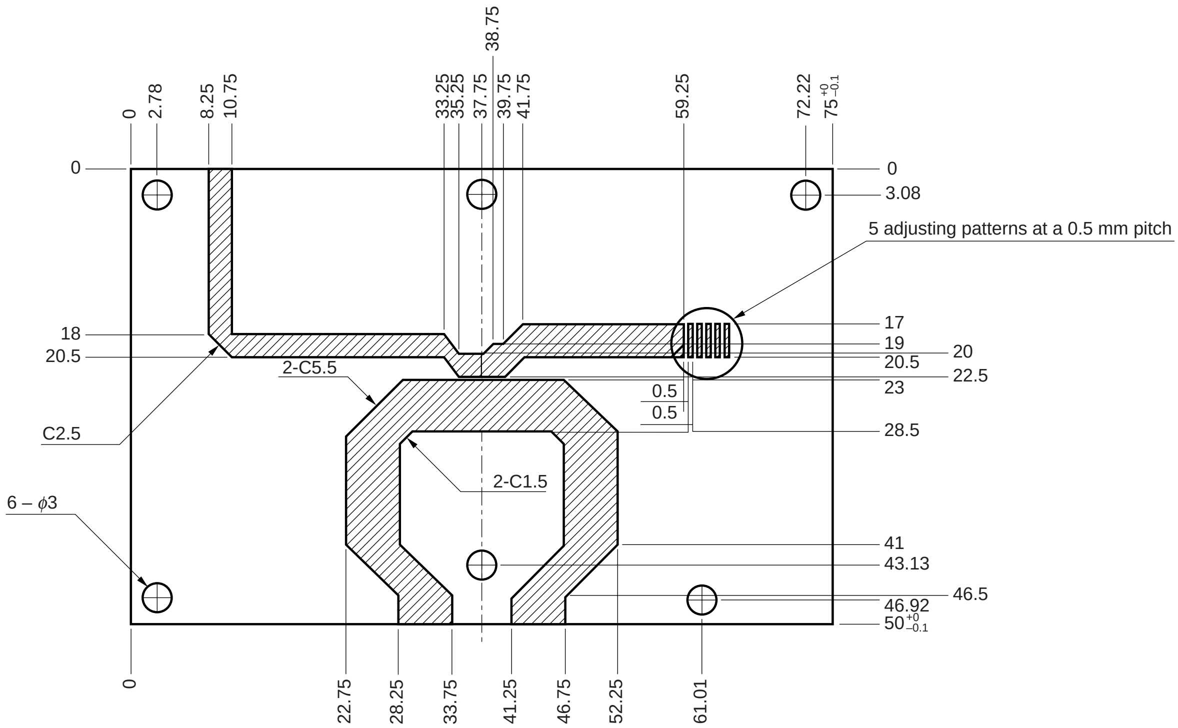
RF TEST FIXTURE



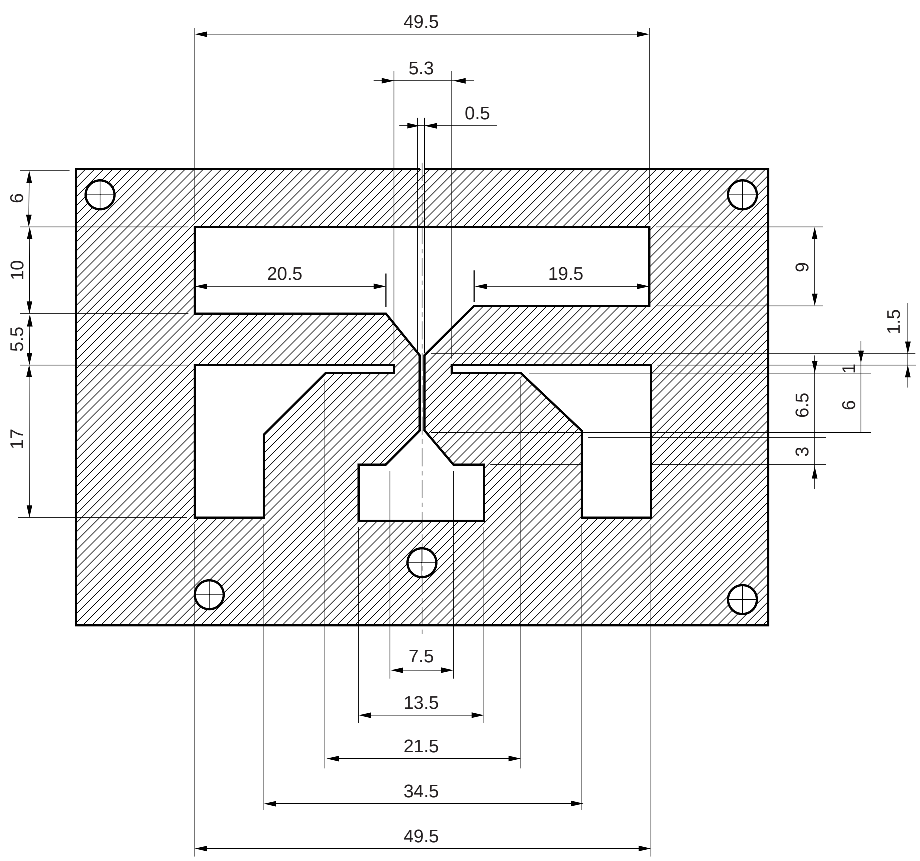


FIGURES OF SUBSTRATE (UNIT: mm)

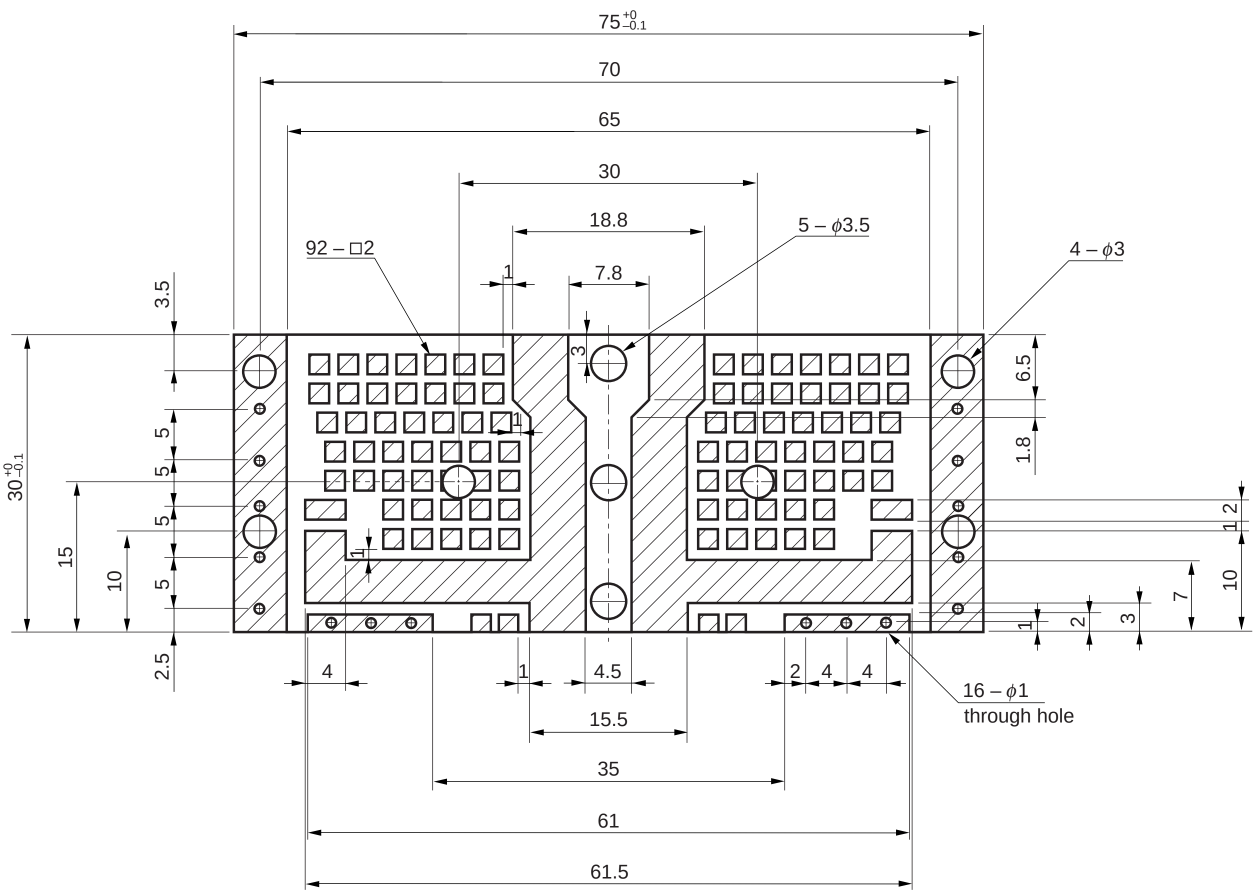
BALUN (FACE)



BALUN (BACK)

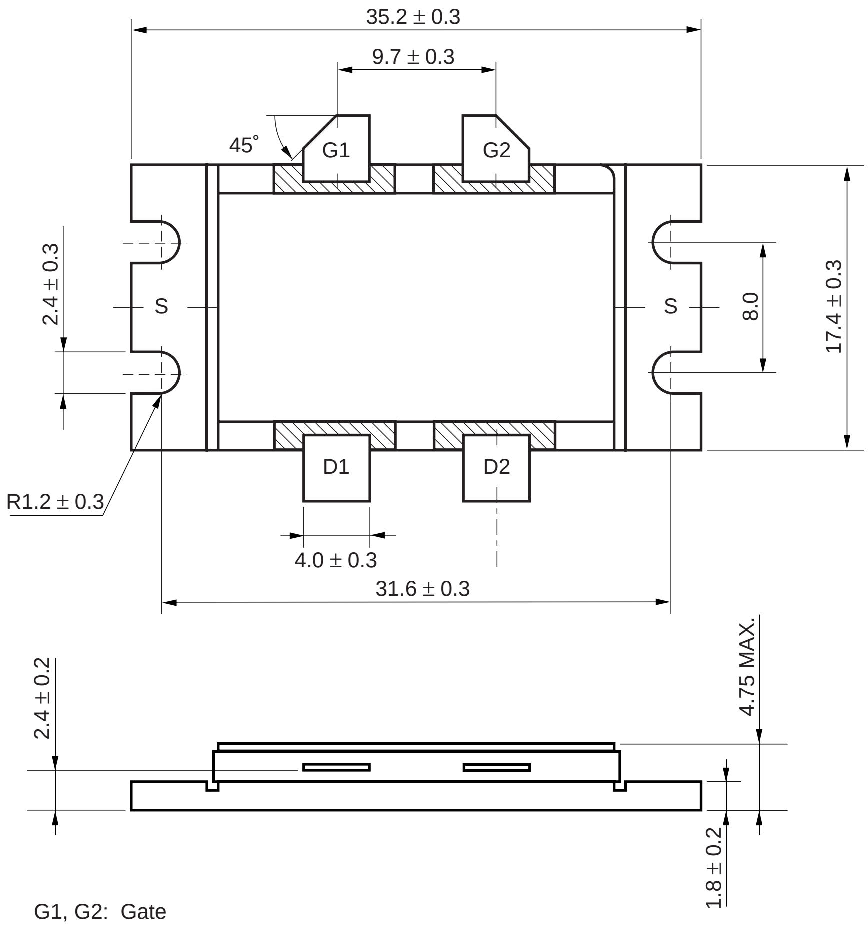


TRANSFORMER



t = 0.8 mm
ε_r = 2.2

PACKAGE DIMENSIONS (UNIT: mm)



G1, G2: Gate
D1, D2: Drain
S : Source

RECOMMENDED MOUNTING CONDITION FOR CORRECT USE

(1) Fix to a heatsink or mount surface completely with screw at the four holes of the flange.
(2) Recommended torque strength of the screw is 3 kgF typical using M2.3 type screw.
(3) Recommended flatness of the mount surface is less than ±10 μm. (roughness of surface is ▽▽▽)

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Partial Heating	Pin temperature: 260°C Time: 5 seconds or less (per pin row)	–

For details of recommended soldering conditions, please contact your local NEC sales office.

[MEMO]

[MEMO]

[MEMO]

Caution

The Great Care must be taken in dealing with the devices in this guide.
The reason is that the material of the devices is GaAs (Gallium Arsenide), which is designated as harmful substance according to the law concerned.
Keep the law concerned and so on, especially in case of removal.