

MOS FIELD EFFECT TRANSISTOR  
 NP40N055CHE, NP40N055DHE, NP40N055EHE, NP40N055KHE

SWITCHING  
 N-CHANNEL POWER MOS FET

DESCRIPTION

These products are N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

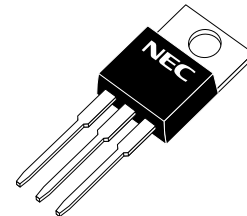
- Channel temperature 175 degree rated
- Super low on-state resistance  
 $R_{DS(on)} = 23 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 20 \text{ A)}$
- Low  $C_{iss}$  :  $C_{iss} = 1070 \text{ pF TYP.}$
- Built-in gate protection diode

ORDERING INFORMATION

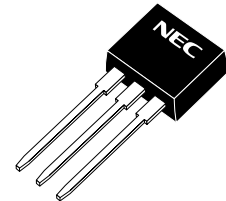
PART NUMBER	PACKAGE
NP40N055CHE	TO-220AB
NP40N055DHE	TO-262
NP40N055EHE	TO-263 (MP-25ZJ)
NP40N055KHE	TO-263 (MP-25ZK)

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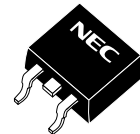
(TO-220AB)



(TO-262)



(TO-263)



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage	$V_{DS}$	55	V
Gate to Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 40$	A
Drain Current (Pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 100$	A
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_T$	1.8	W
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_T$	66	W
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	$-55 \text{ to } +175$	$^\circ\text{C}$
Single Avalanche Current <sup>Note2</sup>	$I_{AS}$	29 / 21 / 7	A
Single Avalanche Energy <sup>Note2</sup>	$E_{AS}$	0.8 / 44 / 49	mJ

Notes 1.  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1\%$

2. Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 28 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$  (See Figure 4.)

THERMAL RESISTANCE

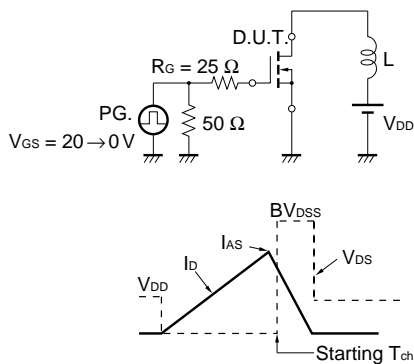
Channel to Case Thermal Resistance	$R_{th(ch-C)}$	2.27	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

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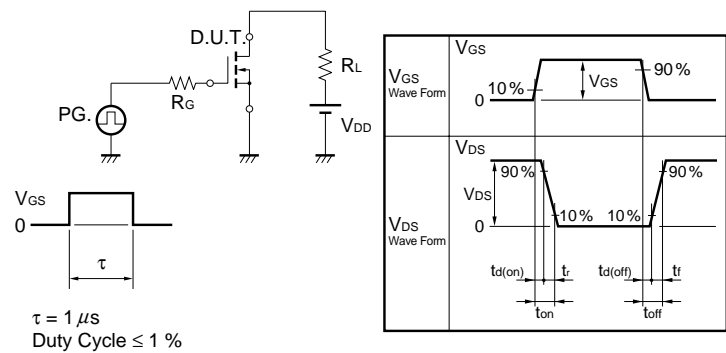
ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		18	23	mΩ
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	3.0	4.0	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 20 A	7	14		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 55 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V		1070	1610	pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		190	280	pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		95	180	pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 20 A		16	35	ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V		9.2	23	ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 28 V		29	57	ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 1 Ω		9.2	23	ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 40 A		23	35	nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 44 V		6		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 10 V		9		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0 V		1.0		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0 V		38		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		46		nC

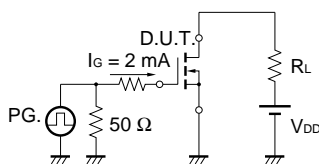
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

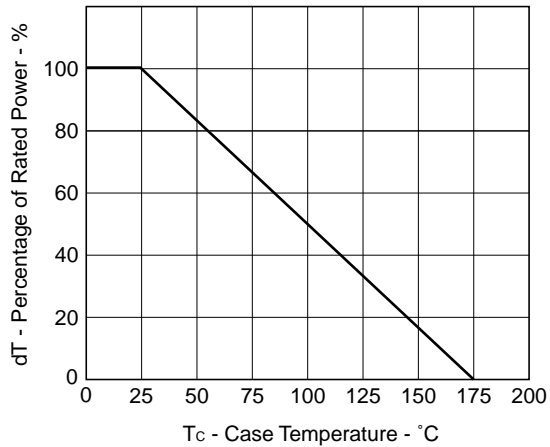


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

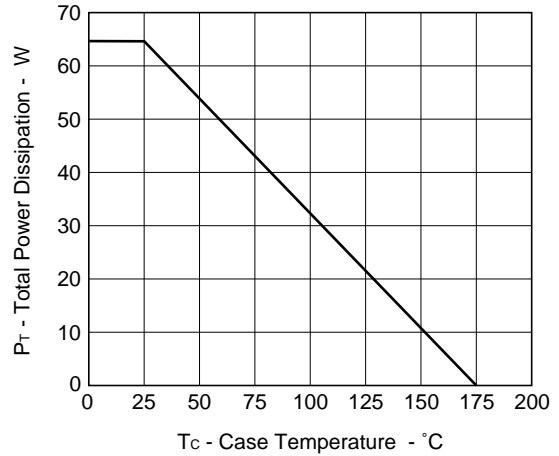


Figure3. FORWARD BIAS SAFE OPERATING AREA

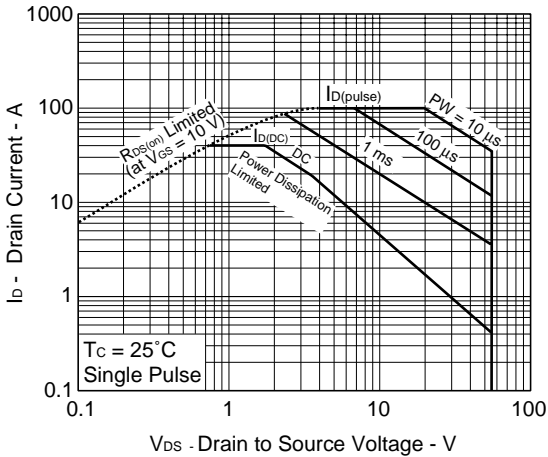


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR

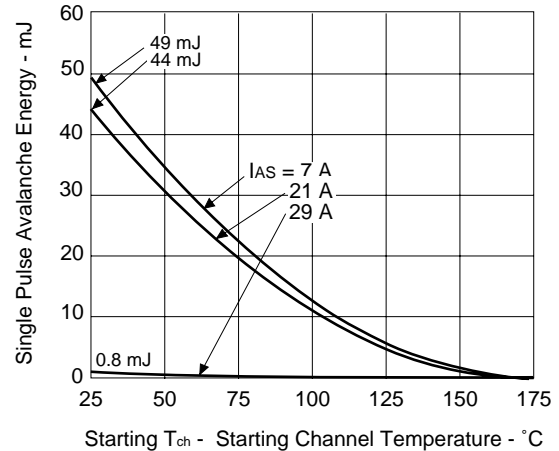


Figure5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

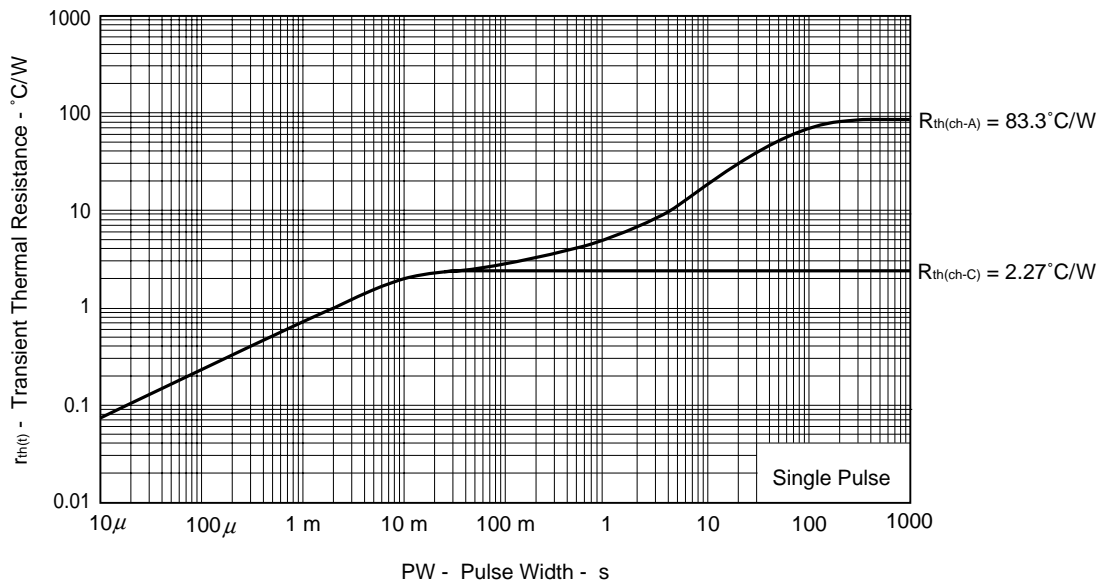


Figure6. FORWARD TRANSFER CHARACTERISTICS

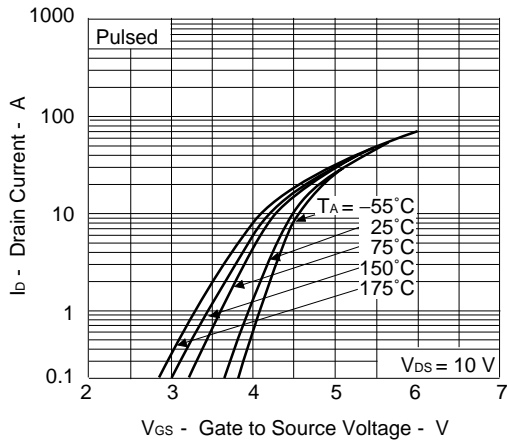


Figure7. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

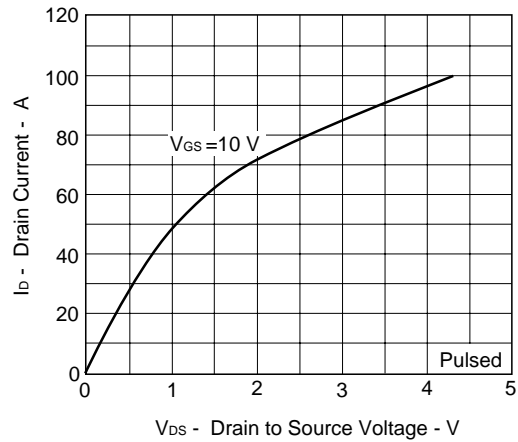


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

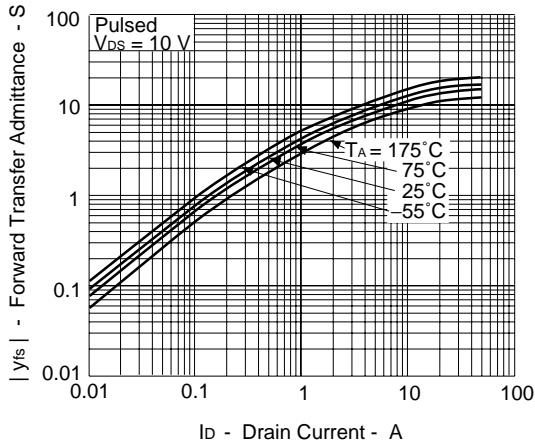


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

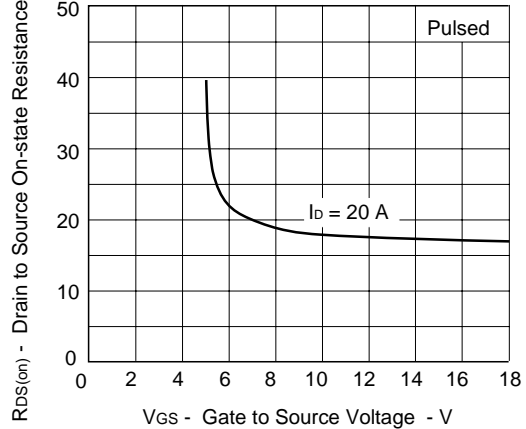


Figure10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

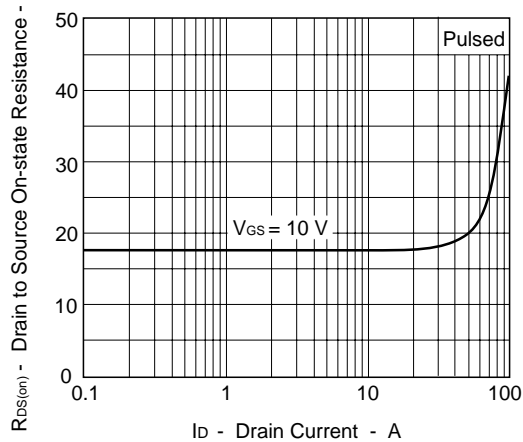


Figure11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

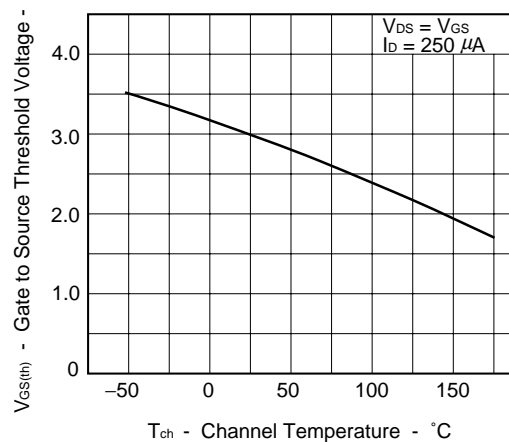


Figure12. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

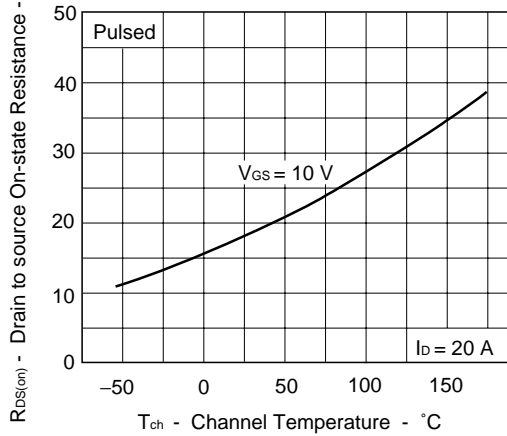


Figure13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

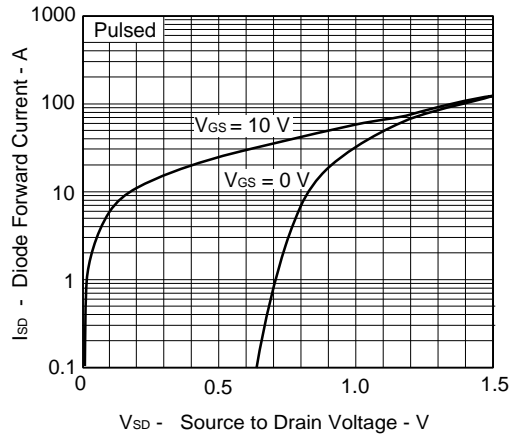


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

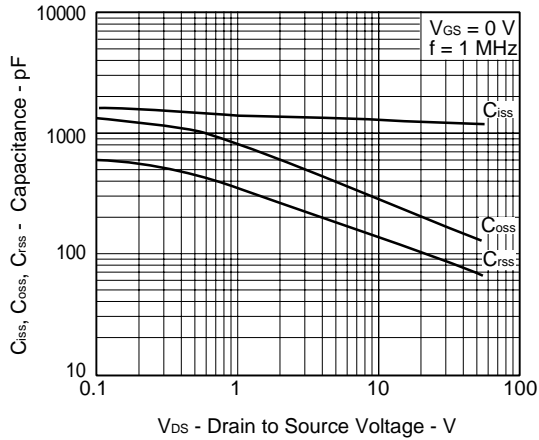


Figure15. SWITCHING CHARACTERISTICS

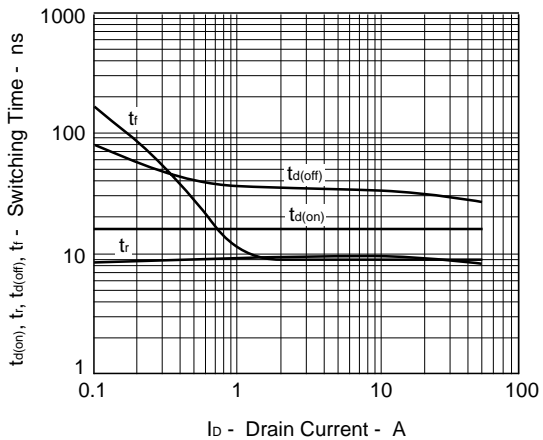


Figure16. REVERSE RECOVERY TIME vs. DRAIN CURRENT

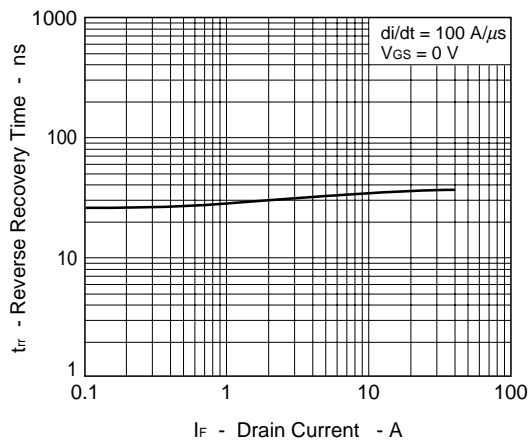
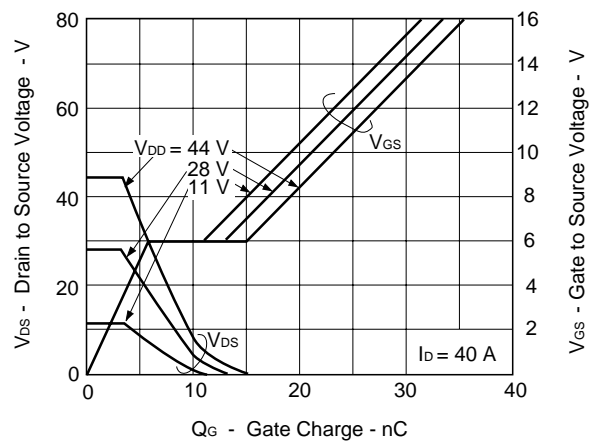
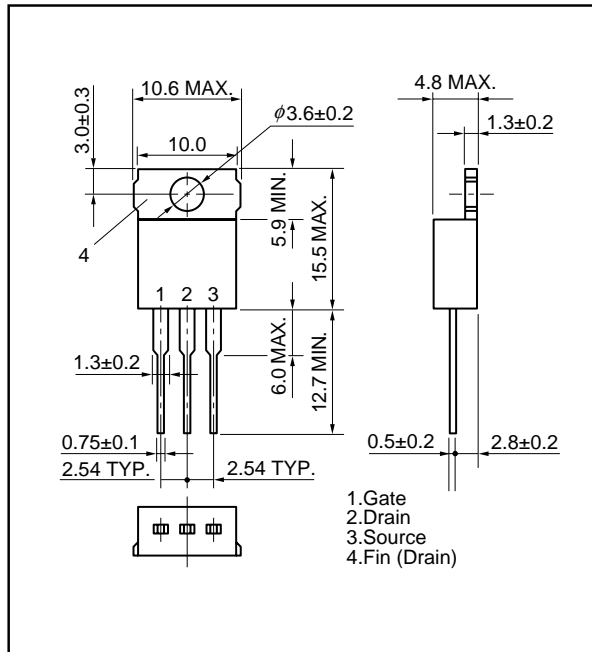


Figure17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

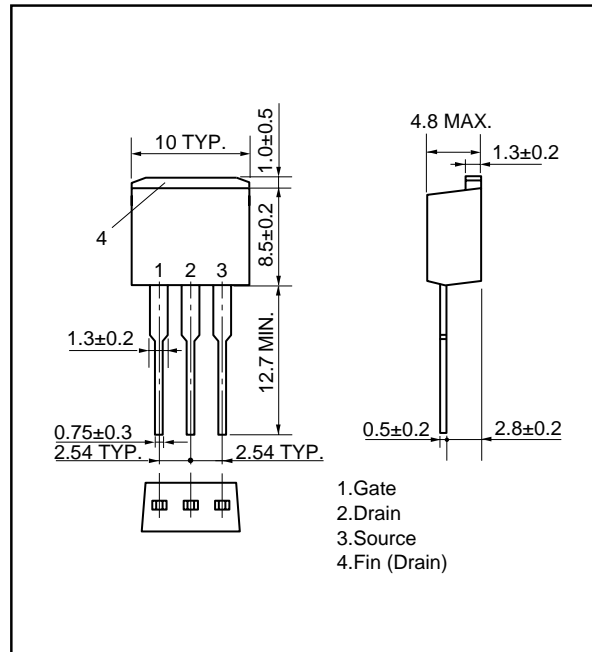


PACKAGE DRAWINGS (Unit: mm)

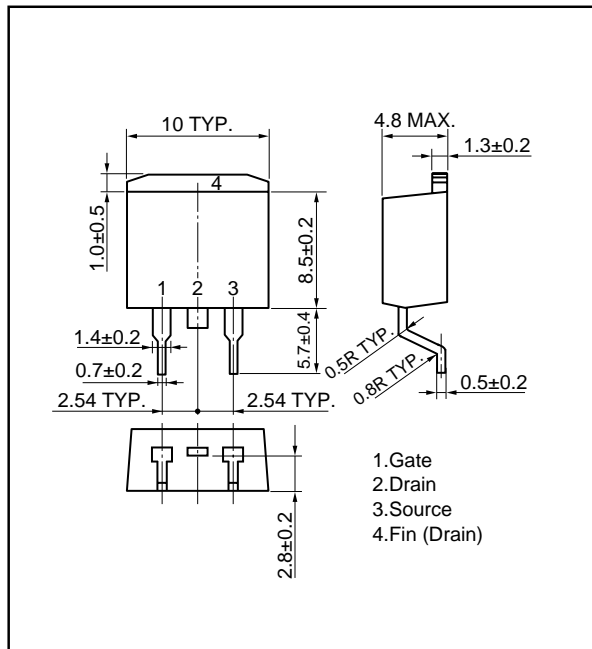
1) TO-220AB (MP-25)



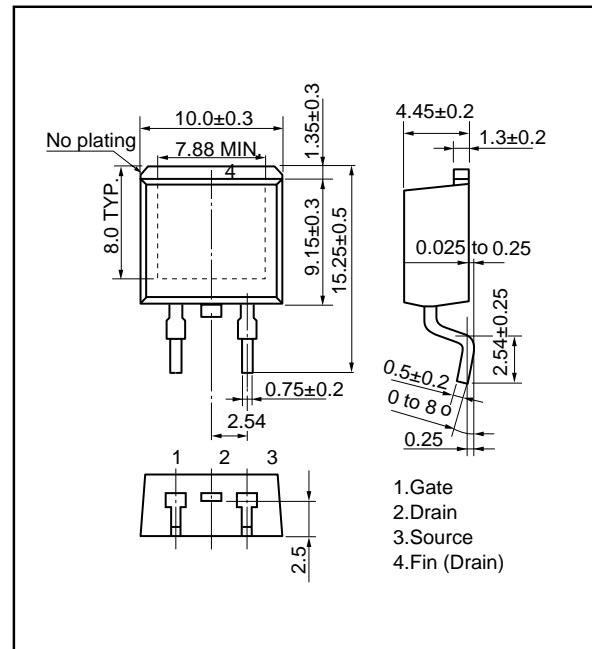
2) TO-262 (MP-25 Fin Cut)



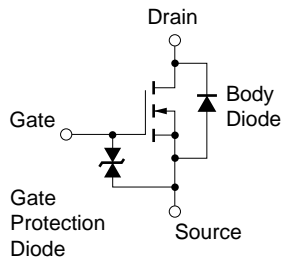
3) TO-263 (MP-25ZJ)



★ 4) TO-263 (MP-25ZK)



**EQUIVALENT CIRCUIT**



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.





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